ACS8514 SETS Buddy

Synchronous Equipment Timing Source Partner IC for
2nd T4 DPLL, Accurate Monitoring & Input Extender

ADVANCED COMMS & SENSING **FINAL** **DATASHEET**

Description

The ACS8514 is an optional partner integrated circuit for applications using the ACS8520/30. It adds an additional BITS clock (T4 path) DPLL to a clock synchronization system, for applications needing two T4 paths (e.g. to GR-253 figure 5-21).

An alternative use for this DPLL is as an input extender such that the ACS8514 automatically selects one of 14 clock sources, its output then feeds the ACS8530/20 which can also select another 13 sources, giving a total input selection range of 27 sources. An additional 13 sources can be added for each ACS8514 added.

An additional highly accurate phase and frequency monitor is also available that can be used to carry out more detailed analysis of standby clock reference sources. This extra monitor is actually another DPLL which under software control could be set to sequentially analyze each input. It can check phase from 0.7° to 23000° and frequency from 0.0003ppm to 80 ppm. An approximate MTIE measurement could be calculated for each reference input as an extra quality check.

Simultaneous activity and coarse frequency monitoring of all input sources is performed in the same way as on the ACS8520/30. These can be used to automatically qualify and select sources for the extra T4 path or for input selection for the ACS8520/30 when the ACS8514 is used as an input extender.

Features

- Partner to the ACS8520 & ACS8530 for use in SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) applications, to provide :
- One Extra independent T4 path for those systems being designed to Figure 5-21 of Bellcore GR253[17],
- An additional DPLL for accurate phase, average phase, frequency and average frequency measuring of any clock source.
- Phase measurement accuracy to 0.7 degrees.
- Frequency measurement accuracy to 3×10^{-10}
- Aids in enhancing Phase Build-out performance to absorb phase disturbances when switching between noisy input sources, via s/w control.
- Provides the facility to have long term frequency measuring and averaging for BOTH the main and any standby clock source so that the holdover frequency is always accurate for both main and standby clock selections.
- Accepts 14 individual input reference clocks, all with robust input clock source quality monitoring.
- Microprocessor interface - Intel, Motorola, Serial, Multiplexed, or boot from EPROM
- IEEE 1149.1[5] JTAG Boundary Scan
- Single 3.3 V operation. 5 V tolerant
- Lead (Pb)-free version available (ACS8514T), RoHS and WEEE compliant

Block Diagram

Figure 1 Block Diagram of the ACS8514 SETS Buddy

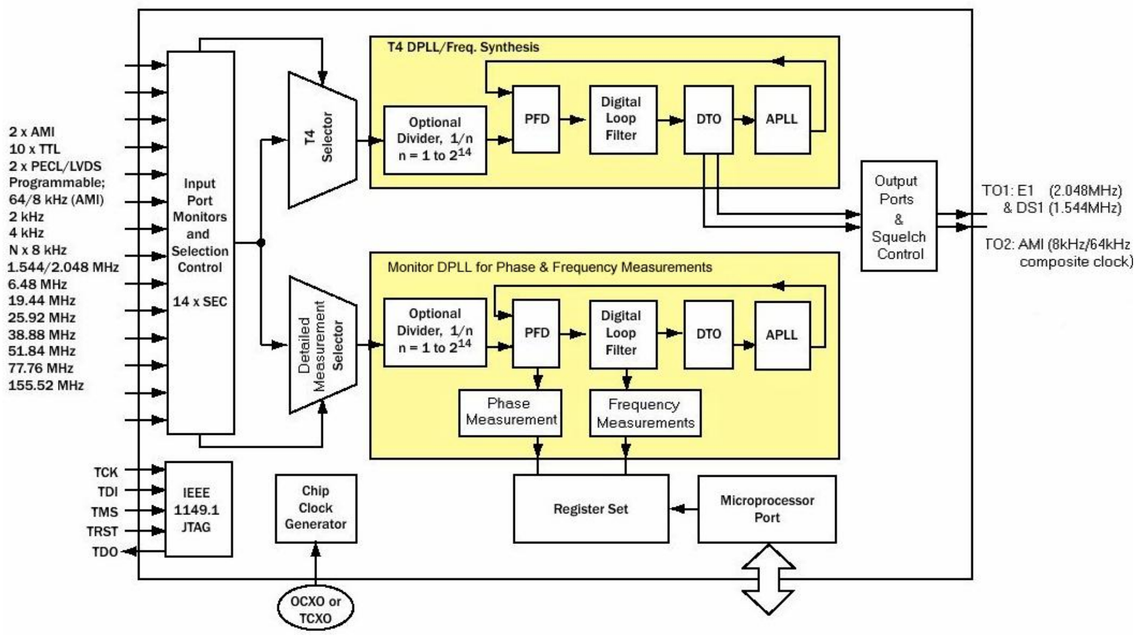

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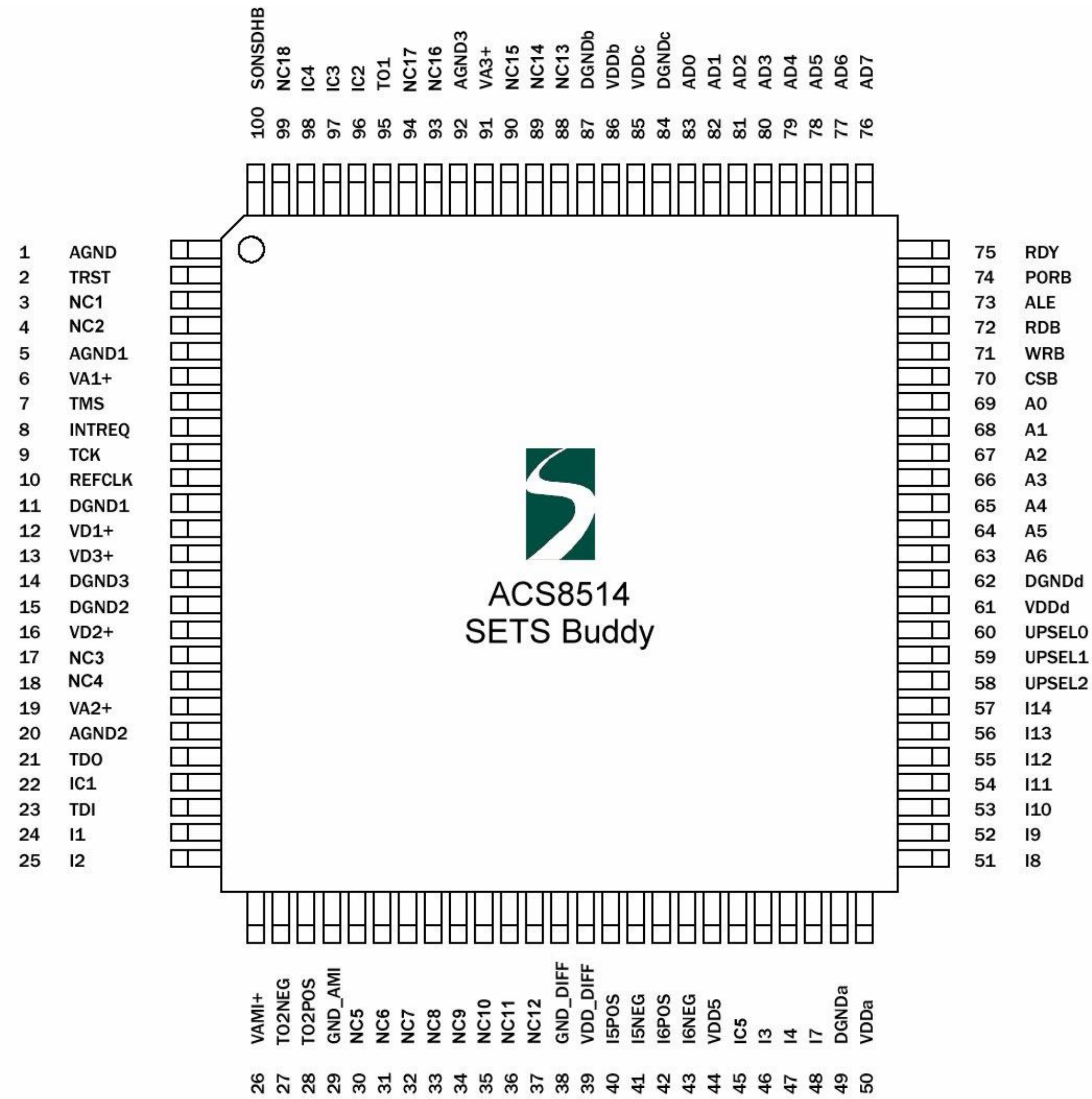
Figure 2 ACS8514 Pin Diagram



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
12, 13, 16	VD1+, VD3+, VD2+	P	-	Supply voltage: Digital supply to gates in analog section, +3.3 Volts ± 10%.
26	VAMI+	P	-	Supply voltage: Digital supply to AMI output, +3.3 Volts ± 10%.
39	VDD_DIFF	P	-	Supply voltage: Digital supply for differential ports, +3.3 Volts ± 10%.
44	VDD5	P	-	VDD5: Digital supply for +5 Volts tolerance to input pins. Connect to +5 Volts (± 10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
50, 61, 85, 86	VDDa, VDDd, VDDc, VDDb	P	-	Supply voltage: Digital supply to logic, +3.3 Volts ± 10%.
6	VA1+	P	-	Supply voltage: Analog supply to clock multiplying PLL, +3.3 Volts ± 10%.
19, 91	VA2+, VA3+	P	-	Supply voltage: Analog supply to output PLLs, +3.3 Volts ± 10%.
11, 14, 15,	DGND1, DGND3, DGND2,	P	-	Supply Ground: Digital ground for components in PLLs.
49, 62, 84, 87	DGNDa,DGNDd, DGNDc,DGNDb	P	-	Supply Ground: Digital ground for logic.
29	GND_AMI	P	-	Supply Ground: Digital ground for AMI output.
38	GND_DIFF	P	-	Supply Ground: Digital ground for differential ports.
1, 5, 20, 92	AGND, AGND1, AGND2, AGND3	P	-	Supply Ground: Analog grounds.

Note: I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected Pins

Pin Number	Symbol	I/O	Type	Description
22, 45, 96, 97, 98	IC1 - IC5	-	-	Internally Connected: Leave to Float.

Table 3 Not connected Pins

Pin Number	Symbol	I/O	Type	Description
3, 4, 17, 18, 30-37, 88–90, 93, 94, 99	NC1 – NC18	-	-	Not Connected Internally : Leave to float or connect to gnd advised, but may be routed over if necessary.

Table 4 Other Pins

Pin Number	Symbol	I/O	Type	Description
2	TRST	I	TTL$_D$	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for Boundary Scan stand-by mode, still allowing correct device operation. If not used connect to GND or leave floating.
7	TMS	I	TTL^U	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL/CMOS	Interrupt Request: Active high/low software Interrupt output.
9	TCK	I	TTL$_D$	JTAG Clock: Boundary Scan clock input. If not used connect to GND or leave floating.
10	REFCLK	I	TTL	Reference Clock: 12.8 MHz (refer to section headed Local Oscillator Clock).
21	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL^U	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
24	I1	I	AMI	Input reference 1: Composite clock 64 kHz + 8 kHz.
25	I2	I	AMI	Input reference 2: Composite clock 64 kHz + 8 kHz.
27	TO2NEG	O	AMI	Output reference 8: Composite clock, 64 kHz + 8 kHz negative pulse.
28	TO2POS	O	AMI	Output reference 8: Composite clock, 64 kHz + 8 kHz positive pulse.
40, 41	I5POS, I5NEG	I	LVDS/PECL	Input reference 5: Programmable, default 19.44 MHz, default type LVDS.
42, 43	I6POS, I6NEG	I	PECL/LVDS	Input reference 6: Programmable, default 19.44 MHz, default type PECL.
46	I3	I	TTL$_D$	Input reference 3: Programmable, default 8 kHz.
47	I4	I	TTL$_D$	Input reference 4: Programmable, default 8 kHz.
48	I7	I	TTL$_D$	Input reference 7: Programmable, default 19.44 MHz.
51	I8	I	TTL$_D$	Input reference 8: Programmable, default 19.44 MHz.
52	I9	I	TTL$_D$	Input reference 9: Programmable, default 19.44 MHz.
53	I10	I	TTL$_D$	Input reference 10: Programmable, default 19.44 MHz.
54	I11	I	TTL$_D$	Input reference 11: Programmable, default (Master mode) 1.544/2.048 MHz, default (Slave mode) 6.48 MHz.
55	I12	I	TTL$_D$	Input reference 12: Programmable, default 1.544/2.048 MHz.
56	I13	I	TTL$_D$	Input reference 13: Programmable, default 1.544/2.048 MHz.
57	I14	I	TTL$_D$	Input reference 14: Programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL$_D$	Microprocessor select: Configures the interface for a particular microprocessor type at reset.
63 - 69	A(6:0)	I	TTL$_D$	Microprocessor Interface Address: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode - output in EPROM mode only.

Table 4 Other Pins (continued)

Pin Number	Symbol	I/O	Type	Description
70	CSB	I	TTL^U	Chip Select (Active Low): This pin is asserted Low by the microprocessor to enable the microprocessor interface - output in EPROM mode only.
71	WRB	I	TTL^U	Write (Active Low): This pin is asserted Low by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL^U	Read (Active Low): This pin is asserted Low by the microprocessor to initiate a read cycle.
73	ALE	I	TTL_D	Address Latch Enable: This pin becomes the address latch enable from the microprocessor. When this pin transitions from High to Low, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL^U	Power On Reset: Master reset. If PORB is forced Low, all internal states are reset back to default values.
75	RDY	O	TTL/CMOS	Ready/Data acknowledge: This pin is asserted High to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	IO	TTL_D	Address/Data: Multiplexed data/address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode.
95	TO1	O	TTL/CMOS	Output reference 9: 1.544/2.048 MHz, as per ITU G.783[9] BITS requirements.
100	SONSDHB	I	TTL_D	SONET or SDH frequency select: Sets the initial power up state (or state after a PORB) of the SONET/SDH frequency selection registers, see register address 34h, Bit 2 and address 38h, Bit 5 & 6 and address 64h, bit 4. When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power up by software.

Introduction

The ACS8514 is a highly integrated multiple phase lock loop device designed to partner the ACS8530 and ACS8520 SETS (Synchronous Equipment Timing Source) ICs. It specifically provides one additional BITS / T4 Path to allow a complete clock synchronization system to have two totally independent T4 paths and one T0 path, for those systems constructed to exactly match the configuration as defined in GR253 figure 5-21.

The electrical interfaces for input clocks, configurations and micro-processor interfaces are identical to the ACS8520/30. This allows the same processor interface pins to be shared with this part, with the correct part accessed by using a separate chip select.

All 14 input clocks and the 12.8 MHz TCXO/OCXO system clock can also be shared via parallel connections.

An alternative use for this part is as an input extender for those systems requiring a selection of more than 14 inputs, or more inputs of a particular electrical interface type. The 14 in-built activity monitors and frequency monitors can automatically qualify an input clock and select that clock based on a preset priority. The T4 DPLL output can then be fed on to the ACS8520/30 for subsequent selection according to its priority tables, as required.

The third main set of functions that this part brings to a system is the capability to very precisely measure the phase and frequency at the inputs. Another independently controlled 'monitor DPLL' can be used for this function. This precise measurement capability can measure phase to a 0.7 degrees accuracy with a range up to 23000° degrees and frequency to 0.3 parts per billion (3×10^{-10}), this is in addition to the activity monitoring and coarse frequency monitoring that occurs simultaneously on each of the 14 input pins to a 3.9 ppm frequency accuracy. The measured phase values may be used to give a TIE (Time Interval Error), MTIE (Maximum TIE) and TDEV (Time Deviation) quality assessment of each input using appropriate external software. The phase and frequency measurement DPLL, the Monitor DPLL, can be set to a range of loop bandwidths, down to 0.5 mHz. The phase of an input is measured with respect to the Monitor DPLL output, so varying the DPLL's bandwidth has the effect of changing the maximum observation time for the TIE measurements. A TIE observation period of up to approximately 2000 seconds is allowed for with the 0.5 mHz bandwidth.

Longer observation time measurements of TIE, MTIE and TDEV can be made by using the T4 DPLL since the T4 phase detectors can be configured to measure the phase difference between two independent inputs. This means that there is no limit to the maximum observation time that can be measured.

A Digital Phase Locked Loop (DPLL) incorporating direct digital synthesis (DDS) is used in the device in order to perform frequency translation. This enables the ACS8514 to have overall PLL characteristics that are very stable and consistent, compared to traditional analog PLLs.

In the absence of any input clock after power up the ACS8514 will free-run and generate a stable, low-noise clock signal at a frequency to the same accuracy as the external 12.8 MHz TCXO or OCXO, or it can be made more accurate via software calibration to 0.02 ppm.

Once an input clock source becomes available and is measured and found to be of a good quality, the T4 DPLL will lock to the source with the highest priority (number 1 is the highest priority in the priority table). If all sources subsequently fail then either the last source frequency is held on the T4 DPLL output (holdover) or the output may be automatically turned off (squelched) depending on configuration.

An internal analog PLL (APLL) is used in the feedback path of the DPLLs in order to eliminate digital sampling effect uncertainty at the DPLL PFDs (Phase and Frequency Detectors).

The ACS8514 includes a multi-standard microprocessor port, providing access to the configuration and status registers for device setup and monitoring.

General Description

Overview

The following description refers to the Block Diagram (Figure 1 on page 1).

The ACS8514 SETS device has 14 input clocks and generates 2 output clocks derived from the T4 DPLL path. Of the 14 input references, two are AMI composite clock, two are LVDS/PECL and the remaining ten are TTL/CMOS compatible inputs. All the TTL/CMOS are 3 V and 5 V compatible (with clamping if required by connecting the VDD5 pin). The AMI inputs are ±1 V typically, A.C. coupled. Refer to the electrical characteristics section for more information on the electrical compatibility and details. Input frequencies supported range from 2 kHz to 155.52 MHz.

Common E1, DS1, OC3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz, can also be locked to via an inbuilt programmable divider.

An input reference monitor is assigned to each of the 14 inputs. The monitors operate continuously such that at all times the status of all of the inputs to the device is known. Each input can be monitored for both frequency and activity, activity alone, or the monitors can be disabled.

The frequency monitors have a "hard" (rejection) alarm limit and a "soft" (flag only) alarm limit for monitoring frequency. Each input reference can be programmed with a priority number allowing references to be chosen according to the highest priority valid input. The input selection can operate in either automatic mode or external manual source selection mode.

The T4 PLL path supports the following features:

- Automatic source selection according to input priorities and quality level.
- Different quality levels (activity alarm thresholds) for each input
- Variable bandwidth (18, 35 or 70 Hz), lock range (0 – 80 ppm) and damping factor.
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Automatic locking to an available source and either squelch or holdover mode when no source.
- Fast detection on input failure.
- Output holds last frequency (holdover) or output squelch when all input sources failed.
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics..
- Ability to measure a phase difference between two inputs.
- Analog PLL (APLL) used in the feedback path to avoid digital sampling / aliasing effects.

Either external software or an internal state machine controls the T4 DPLL source selection based on input quality and priority.

Input Reference Clock Ports

Table 4 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown. Note that SDH and SONET networks use different default frequencies; the network type is pin-selectable (using either the SONSDHB pin or via software). Specific frequencies and priorities are set by configuration.

SDH and SONET networks use different default frequencies; the network type is selectable using the register bit *ip_sonsdhb*, at address 34, bit 2.

- For SONET, *ip_sonsdhb* = 1
- For SDH, *ip_sonsdhb* = 0

On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 100).

The specific frequency selection is programmed via the *cnfg_ref_source* registers (addresses 22 to 2D).

Locking Frequency Modes

There are three locking frequency modes that can be configured: Direct Lock, Lock 8k and DivN.

Direct Lock Mode

In Direct Lock Mode, the internal DPLL can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes (and for special case of 155 MHz), an internal divider is used prior to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies (see Table 1, note 0). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate register location (at address 22 to 2D). Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter. It is possible to choose which edge of the input reference clock to lock to, by setting *8K edge polarity* (Bit 2 of register 03*).*

DivN Mode

DivN mode allows the input to be divided by any integer value. The mode is engaged by bit 7 of registers 22 to 2D allowing any input to use this mode. The divide value is set by register 46 & 47, it must be set so that the frequency after division is 8 kHz.

The DivN function is defined as :

DivN = "Divide by (N+1)", i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N+1) where N is an integer from 1 to 12499 inclusive, as set by registers 46 & 47h.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 12500. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz to 100 MHz, can be supported by using DivN mode.

Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs. However only one value of N is allowed, so all inputs with DivN selected must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the cnfg_ref_source_frequency register (address 22 - 2D) to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN=250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair at address 46 & 47.

(b) To lock to 10.000 MHz:

(i) The cnfg_ref_source_frequency register (address 22 - 2D) is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair at address 46 & 47.

Direct Lock Mode 155 MHz.

The max frequency allowed for phase comparison is 77.76 MHz, so for the special case of a 155 MHz input set to Direct Lock Mode, there is a divide-by-two function automatically selected to bring the frequency down to within the limits of operation.

PECL/LVDS/AMI Input Port Selection

The choice of PECL or LVDS compatibility is programmed via the cnfg_differential_inputs register, address 36h. Unused PECL differential inputs should be fixed with one input High (VDD) and the other input Low (GND), or set in LVDS mode and left floating, in which case one input is internally pulled High and the other Low .

An AMI port supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[6]. Departures from the nominal pattern are detected within the ACS8514, and may cause reference-switching if too frequent. See section DC Characteristics: AMI Input/Output Port, for more details. If the AMI port is unused, the pins (I1 and I2) should be tied to GND.

Table 5 Input Reference Source Selection and Priority Table for T4 DPLL

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I1	0001	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	0
I2	0010	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	0
I3	0011	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 8 kHz Default (SDH): 8 kHz	0
I4	0100	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 8 kHz Default (SDH): 8 kHz	0
I5	0101	LVDS/PECL LVDS default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	6

Port Number	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
I6	0110	PECL/LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	7
I7	0111	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	8
I8	1000	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	9
I9	1001	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	10
I10	1010	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	11
I11	1011	TTL/CMOS	Up to 100 MHz (see Note 0) Default (Master) (SONET): 1.544 MHz Default (Master) (SDH): 2.048 MHz Default (Slave) 6.48 MHz	12
I12	1100	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	0
I13	1101	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	0
I14	1110	TTL/CMOS	Up to 100 MHz (see Note 0) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	0

Notes:

(i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH input rate is selected via register 34 bit 2, ip_sonsdhb).

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz.

Clock Quality Monitoring

Clock quality is monitored and used to modify the priority tables of the local and remote ACS8520/30 devices. The following parameters are monitored continuously for all 14 inputs in parallel :

1. Activity (toggling).
2. Frequency to +/- 3.8 ppm accuracy (this monitoring is only performed when there is no irregular operation of the clock or loss of clock condition).

A fine level of frequency monitoring and phase monitoring is also performed in the two DPLLs. Phase is measured down to 0.7 degrees with a maximum range of +/- 8191 cycles or +/- 2.9 x 10^6 degrees. Frequency is measured to a 0.0003 ppm resolution and +/- 80 ppm range (could be up to +/- 500 ppm with software enhanced use of the calibration register (3Ch, 3Dh).

Input ports I1 and I2 carry AMI-encoded composite clocks which are also additionally monitored by the AMI-decoder blocks. Loss of signal is declared by the decoders when either the signal amplitude falls below +0.3 V or there is no activity for 1 ms.

Any reference source that suffers a loss-of-activity or clock-out-of-band condition will be declared as unavailable.

Activity Monitoring

The ACS8514 tests for too much or too little activity via the activity monitors. The ACS8514 uses a Leaky Bucket Accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the output amplitude but die away over time. Such integrators are used when alarms have to be triggered either by fairly regular defect events, which occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By adjusting the alarm setting threshold, the point at which the alarm is triggered can be controlled. The point at which the alarm is cleared depends upon the decay rate and the alarm clearing threshold.

On the alarm setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). See Figure 3 .

There is one Leaky Bucket Accumulator per input channel. Each Leaky Bucket can select from one of four Configurations (Leaky Bucket Configuration 0 to 3). Each Leaky Bucket Configuration is programmable for size, alarm set and reset thresholds, and decay rate.

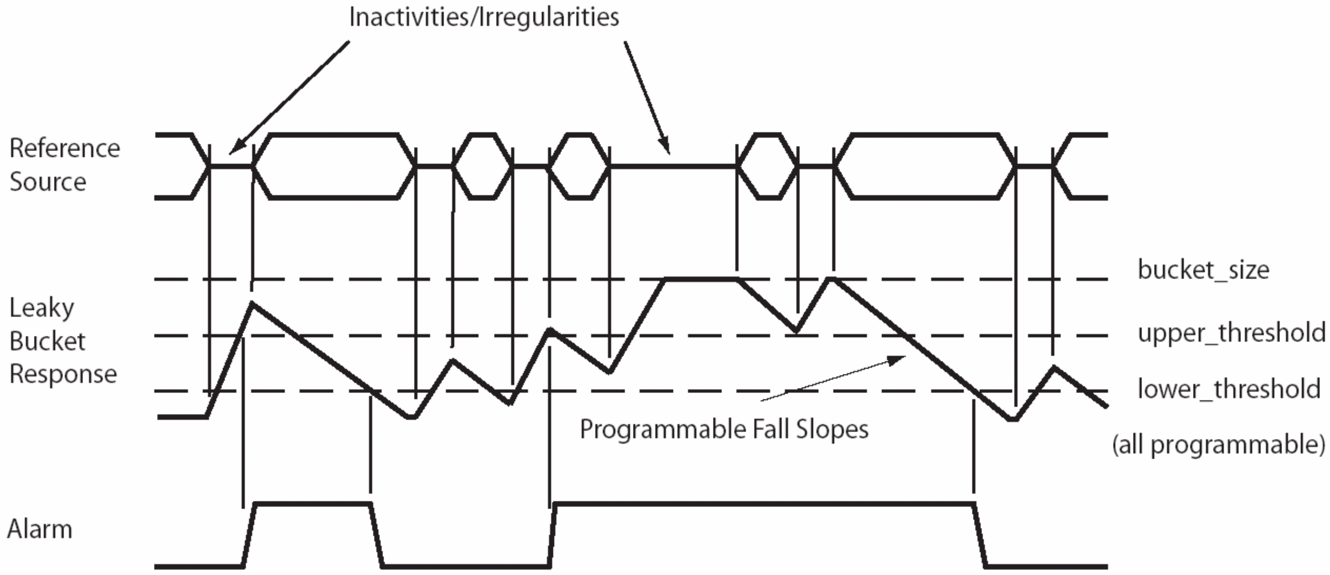
Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the Accumulator is incremented. Irregularity is defined as too much or too little activity (corresponding to +/- 1000ppm on a frequency basis).

The Accumulator will continue to increment up to the point that it reaches the programmed Bucket size. The "fill rate" of the Leaky Bucket is, therefore, 8 units/second. The "leak rate" of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to "leak" at the same time as a "fill" is avoided by preventing a leak when a fill event occurs.

Disqualification of a non-selected reference source is based on inactivity, or on an out-of-band result from the frequency monitors. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, qualified reference source is selected.

To avoid the DPLL being pulled off by clock inactivity on a shorter timescale than 128ms, the DPLL contains a fast activity detector such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in holdover mode, holding the last output frequency value. With the DPLL in holdover mode it is isolated from further disturbances. If the input

Figure 3 Inactivity and Irregularity Monitoring



becomes available again before the activity or frequency monitor rejection alarms have been raised, then the DPLL will continue to lock to the input, with little disturbance. In this scenario, with the DPLL in the "locked" state, the DPLL uses "nearest edge locking" mode (±180° capture) avoiding cycle slips or glitches caused by trying to lock to an edge 360° away, as would happen with traditional PLLs.

Interrupts for Activity Monitors

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the Leaky Bucket Configuration of the activity monitors. The fastest Leaky Bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the mon_ref_failed interrupt (register 06, bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The pin will, therefore, remain high until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to register 48, bit 6.

Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on a reference source that has previously been fully active (Leaky Bucket empty) will be:

(cnfg_upper_threshold_n) / 8

where n is the number of the Leaky Bucket Configuration. If an input is intermittently inactive then this time can be longer. The default setting of cnfg_upper_threshold is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive reference source is calculated, for a particular Leaky Bucket, as:

$[2^{(a)} \times (b - c)] / 8$

where:

a = *cnfg_decay_rate_n*
b = *cnfg_bucket_size_n*
c = *cnfg_lower_threshold_n*
(where n = the number of the relevant Leaky Bucket Configuration in each case).

The default setting is shown in the following:

$[2^{1} \times (8 - 4)] / 8 = 1.0$ secs

Frequency Monitoring

The ACS8514 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range measured with respect to the external TCXO/OCXO clock.

The sts_reference_sources (addresses 10 - 16h) out-of-band alarm for a particular reference source is raised when the reference source is outside the acceptable frequency range. With the default register settings a soft alarm is raised if the drift is outside ±11.43 ppm and a hard alarm is raised if the drift is outside ±15.24 ppm. Both of these limits are programmable from 3.8 ppm up to 61 ppm.

The ACS8514 DPLLs have a programmable lock and capture range frequency limit up to ±80 ppm (default is ±9.2 ppm).

The following sections show the frequency monitor features and corresponding registers:

Coarse frequency monitors:

(i) All 14 inputs measured in parallel to a 3.8 ppm resolution. Measured over a 32 second interval.

(ii) Hard (rejection) alarm limit and soft (flag only) alarm limit set in registers 49h & 4Ah. Alarm flags shown in registers 10 h – 16h.

(iii) Makes measurement relative to external TCXO/OCXO (Must set register 48h, bit7 to ‘1’).

(iv) Reports measured frequency in register 4Ch. Result selected by register 4Bh.

Monitor DPLL:

(v) Measurement to 0.0003 ppm & +/- 80 ppm range. Result at register 0Ch, 0Dh &07h. Register 4Bh, bit 4 at ‘0’ gives monitor DPLL result. Bit 4 at ‘1’ gives T4 DPLL result.

(vi) Measurement Result may be offset or calibrated by registers 3Ch & 3Dh to +/- 500 ppm.

Both the monitor DPLL and the T4 DPLL can be used as a frequency meter. The frequency value measured and reported by the DPLLs corresponds to the integral path value in the DPLLs. As such it is a filtered version of the actual input frequency. The time constant of the filtering is inversely proportional to the DPLL bandwidth. The value is a 19-bit signed number with one LSB representing 0.0003068 ppm (range of ±80 ppm). Reading this regularly can show how the currently locked source is varying in value e.g. due to frequency wander on its input.

Frequency Averagers

Modes are included to provide additional internal filtering on the frequency value from the monitor DPLL. It would also be possible to combine the internal averaging filters with some additional software filtering. For example, the internal fast filter could be used as an anti-aliasing filter and the software could further filter this before determining the actual average frequency. To support this feature, a facility to read out the internally averaged frequency has been provided. By setting register 40h, bit 5, the value read back from the cnfg_average_frequency register (register 3E, 3F, 40) will be the filtered value.

The amount of filtering applied is set by register 40h, bits 6 & 7 and gives additional filter poles of 8 minutes or 110 minutes.

An Example:

Select fast holdover averaging mode by setting register 40h bits 6 & 7 high.

Select to be able to read back filtered output by setting register 40h bit 5 high.

Software reads averaged value from the cnfg_average_ frequency register at address 3Eh, 3Fh & 40h. All bytes of a multi-byte value such as this are frozen internally until all bytes have been read, or until the same byte is read again, in order to correctly build up the multi byte word.

Phase Monitoring

The T4 DPLL will be monitoring the phase of its selected source with respect to its own output and frequency with respect to a calibrated (see register 3Ch, 3Dh) version of the external 12.8 MHz TCXO.

When register 65h, bit 7 is set to ‘1’ the phase detector from T4 DPLL is used to measure the phase between the selected input for the T4 DPLL (set either by priorities in registers 18h to 1Eh or register 35h, bits 3:0) and the selected input for the monitor DPLL (set by register 33). The T4 DPLL outputs are then invalid since the PLL feedback loop is removed.

The monitor DPLL will also be monitoring the phase of its selected source with respect to its own internal output and frequency with respect to a calibrated (see register 3Ch, 3Dh) version of the external 12.8 MHz TCXO. The input phase, as seen at the DPLL phase detector, can be read back from register 77h and 78h. The reporting of the monitor DPLL or T4 DPLL phase detector value is controlled by register 4Bh, bit 4. One LSB corresponds to approximately 0.7 degrees phase difference.

The phase between two inputs may be measured by by the monitor DPLL by switching from source A to source B and recording the measured phase, first at source A (which will be near to zero if the PLL has had time to pull in) and then at source B. Measuring the phase value 30 ms after source B is selected allows enough time for an average phase measurement to be made and reported to register 77h & 78h, but it is before the DPLL loop has had time to pull in the phase back to zero. It is beneficial to set the DPLL bandwidth to the lowest value (e.g. 0.1 Hz when TCXOs used or down to 0.5 mHz with sufficiently stable OCXOs) to slow the rate of this pull-in.

An averaging filter is used in the phase measurement block to get an accurate value. The bandwidth of this filter is 100 Hz (when DPLL bandwidth at 0.5m Hz to 35 Hz) or 200 Hz (when DPLL bandwidth at 70 Hz). Hence around 30 ms is enough for a settled phase value, although this will depend on the magnitude of the phase change.

Using the above method a phase measurement could be made between the most accurate clock source in a system, which would be from an ACS8530 clock output, and any other input clock, such that TIE, MTIE and TDEV could be subsequently calculated by software.

Alternatively the frequency of a selected source could be monitored with respect to the external TCXO/OCXO, as a way of deriving the TIE, MTIE and TDEV result. It may be that the external OCXO is the most stable reference in a system and therefore the most appropriate for input comparisons. A higher monitor DPLL bandwidth of, for example 8 Hz, would allow input wander to be measured, separate from input jitter which would be filtered out according to the setting of the DPLL bandwidth. The frequency accuracy of 0.0003ppm corresponds to a rate of change of phase accuracy of 0.3 ns per second.

The monitor DPLL could be used for accurate analysis of the standby clock sources and the T4 DPLL left to provide the additional T4 path in a system.

Selection of Input Reference Clock Source

The input reference sources for the T4 DPLL may be selected automatically by an order of priority (via registers 18h to 1Eh, register 4Bh, bit4 must be set to '1'). Alternatively it can be forced by external software control (registers 35h, bits 3:0).

The phase and frequency monitor DPLL has its source selected by external control via register 33h, bit 3:0.

Automatic operation selects a reference source based on its pre-defined priority and its current availability. A table is maintained which lists all reference sources in the order of priority. This is initially defined by the default configuration and can be changed via the microprocessor interface by the network manager. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, the next-highest source is selected, and so on.

The T4 DPLL always operates in revertive mode such that if a valid source has a higher priority than the currently selected reference, a switch over will take place.

Forced Control Selection

For the T4 DPLL register 35 controls both the choice of automatic or forced selection and the selection itself. For automatic choice of source selection, the 4 LSB bit value is set to all zeros. To force a particular input (I_n) , the bit value is set to n (bin).

For the monitor DPLL register 33 controls input selection choice. The power up default has the 4 LSB bit value set to all ones, whereby the DPLL will select the first valid source. The register should be set to a value from 1 to 14 to select the required input for monitoring.

Automatic Control Selection

When an automatic T4 DPLL selection is required, (see above), the priority for each input should be uniquely set in registers 18h to 1Eh (make sure register 4B, bit 4 = 1). Each register holds a 4-bit value which represents the desired priority of that particular port. Unused ports should be given the value, 0000, in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 5. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number; the valid values are 1 to 15 (dec). A value of zero disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis.

Modes of Operation

The T4 DPLL in the ACS8514 has three internal modes of operation: Free-run, Locked and Holdover. Only locked or not locked is reported in a status register (register 09, bit6).

After power up and before any sources become qualified and selected the T4 DPLL will either free run, generating an output frequency to the same accuracy as the external TCXO/OCXO or its output will be squelched, depending on register 64h, bit 6. The accuracy of the external oscillator can be calibrated to appear more accurate via registers 3Ch & 3Dh.

Once the T4 DPLL has locked to a source, then when that source fails, it will hold its last output frequency or its output will be squelched, again depending on register 64 hex, bit 6.

Since the outputs from the monitor DPLL are not accessible its internal output frequency and operating modes are less relevant. Indication as to whether it is locked to a source or not are given in register 09h, bits 2:0.

DPLL Architecture and Configuration

A Digital PLL gives a stable and consistent level of performance that can be easily programmed for different dynamic behavior or operating range. It is not affected by operating conditions or silicon process variations. Digital synthesis is used to generate the required SONET/SDH output frequencies. An analog PLL is used to filter the synthesized digital clock before it is fed back to the DPLL input. This avoids any digital sampling induced wander or jitter.

The DPLLs in the ACS8514 are uniquely very programmable for all PLL parameters of bandwidth (from 0.5 mHz up to 70 Hz), damping factor (from 1.2 to 20), frequency acceptance and output range (from 0 to 80 ppm, typically 9.2 ppm) and input frequency (12 common SONET/SDH spot frequencies). There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly via registers in the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

The T4 DPLL is similar in structure to the monitor DPLL, but its bandwidth is limited to 18, 35 and 70 Hz.

Monitor DPLL Main Features

- Programmable DPLL bandwidth in 10 steps from 0.5 mHz to 70 Hz.
- Programmable damping factor: For optional faster locking. Factors = 1.2, 2.5, 5, 10 or 20.
- Multiple phase lock detectors.
- Multi-cycle phase detection and locking, programmable up to ±8192 UI (readable up to 23000° as a 16 bit register reports the value).
- Input frequency averaging with a choice of averaging times: 8 minutes or 110 minutes.

T4 DPLL Main Features

- E1 (2.048 MHz) or DS1(1.544 MHz) outputs.
- Programmable DPLL bandwidth in 3 steps from 18 Hz to 70 Hz
- Programmable damping factor: For optional faster locking and peaking control. Factors = 1.2, 2.5, 5, 10 or 20
- Multiple phase lock detectors
- Multi-cycle phase detection and locking, programmable up to ±8192 UI - improves jitter tolerance in direct lock mode
- Can use the phase detector in T4 DPLL to measure the input phase difference between two inputs (+/- 0.5UI).

The following sections detail some component parts of the DPLL.

Monitor DPLL Automatic Bandwidth Controls

In Automatic Bandwidth Selection mode (register 3Bh, bit 7), the monitor DPLL bandwidth setting is selected automatically from the Acquisition Bandwidth or Locked Bandwidth configurations programmed in register 69h and 67h respectively. If this mode is not selected, the DPLL acquires and locks using only the bandwidth set by register 67.

Phase Detectors

A Phase and Frequency detector is used to compare input and feedback clocks. This operates at input frequencies up to 77.76 MHz. The whole DPLL can operate at spot frequencies from 2 kHz up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz). A common arrangement however is to use Lock8k mode (See register 22h to 2Dh, Bit 6) where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8514.

A multi-phase detector (patent pending) approach is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. The following phase detectors are used:

- Phase and frequency detector (±360° or ±180° range)
- An Early/ Late Phase detector for fine resolution
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ±360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled and it has detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via register 03h, bit 6 set to 1. In this setting, frequency locking (+/- 360° capture) will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via registers 6Ah to 6Dh. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector is enabled via register 74h, bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI, 3 UI, 7 UI, 15 UI ... up to 8191 UI via register 74, bits [3:0].

When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (register 74h, bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting high, the multi cycle phase value will be used in the loop and gives faster pull in (but more overshoot). The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit low only uses a maximum figure of 360 degrees in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/Loss Detection

Phase lock/loss detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min or max frequency
- Detection of no activity on the input.

Each of these sources of phase loss indication is individually enabled via registers bits (register 73h, 74h and 4Dh) and applies to both the T4 DPLL and the monitor DPLL. Phase lock or lost is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the monitor DPLL. Acquisition bandwidth is used for faster pull in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by register 74h, bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. The ACS8514 provides a choice of damping factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 6 shows which damping factors are available for selection at the different bandwidth settings and what the corresponding jitter transfer approximate gain peak will be.

Table 6 Available Damping Factors for different DPLL Bandwidths, and associated Jitter Peak Values

Bandwidth	Register 6Bh [2:0]	Damping Factor selected	Gain Peak/ dB
0.5mHz to 4 Hz	1, 2, 3, 4, 5	5	0.1
8 kHz	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18 Hz	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Local Oscillator Clock

The Master system clock on the ACS8514 should be provided by an external clock oscillator of frequency 12.8 MHz and may be provided by the same oscillator source as used for the partner ACS8520/30 in a system.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. ±50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8-bit register locations. The setting of the conf_nominal_frequency register (addr 3Ch, 3Dh) allows for this adjustment. An increase in the register value increases the output frequencies by 0.0196229 ppm for each LSB step.

The default register value (in decimal) = 39321 (9999 hex) = 0 ppm offset. The minimum to maximum offset range of the register is 0 to 65535 dec, giving an adjustment range of -771 ppm to +514 ppm of the output frequencies, in 0.0196229 ppm steps.

Example: If the crystal was oscillating at 12.800 MHz + 5 ppm, then the calibration value in the register to give a - 5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be:

39321 - (5/0.0196229) = 39066 (dec) = 989A (hex).

Output Wander & Jitter

Wander and jitter present on the output depends on::

- The magnitudes of wander and jitter on the selected input reference clock (in Locked mode)
- The internal wander and jitter transfer characteristic (in Locked mode). See below.
- The wander on the local oscillator clock (when the T4 DPLL is free running or holding its frequency).

Jitter and Wander Transfer

The T4 DPLL has a programmable jitter transfer characteristic. This is set by the T4 DPLL bandwidth (register 66). The -3 dB jitter transfer attenuation point can be set to 18, 35 or 70 Hz. The wander and jitter transfer characteristic is shown in Figure 4 .

The monitor DPLL has an effective bandwidth of 0.1 to 70 Hz. The setting of bandwidth for this PLL is mainly used to control how quickly the DPLL follows the input source during input phase and frequency measurements. Since the output clock from the monitor DPLL is not accessible, it's transfer characteristic is not measurable.

Wander on the local oscillator clock will not have a significant effect on the T4 DPLL output clock when locked, since the bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal.

In Free-run or frequency holdover wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator.

Input Wander and Jitter Tolerance

The ACS8514 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825[15], ANSI DS1.101-1999[1], Telcordia GR1244, GR253, G812, G813 and ETS 300 462-5 (1997) in terms of jitter tolerance.

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Using either lock8k mode or direct lock mode and the multi UI phase detector, the jitter tolerance limits can set to exceed all tolerance requirements. When the multi UI phase detector is used, the DPLLs can tolerate and track up to +/- 8191 UI. This limit is programmable (see register 74h).

Pull-in, hold-in and pull-out ranges are shown in Table 7.

Table 7 Input Reference Freq range

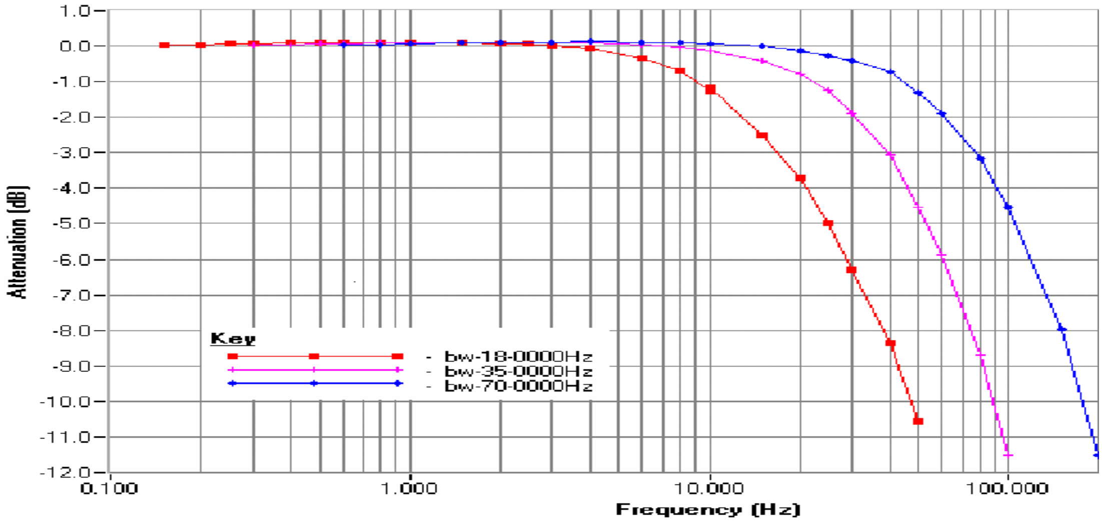
Spec.	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703[6] G.783[9] G.823[13] GR-1244-CORE[19]	±16.6 ppm	±4.6 ppm (Note 0) ±9.2 ppm (Note (i))	±4.6 ppm (Note 0) ±9.2 ppm (Note (i))	±4.6 ppm (Note 0) ±9.2 ppm (Note (i))

Notes:

(i) The frequency acceptance and generation range will be ±4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of ±4.6 ppm.

(ii) The fundamental acceptance range and generation range is ±9.2 ppm with an exact external crystal frequency of 12.800 MHz. This is the default DPLL range; the range is also programmable from 0 to 80 ppm in 0.08 ppm steps.

Figure 4 Measured Jitter Transfer Characteristics T4 DPLL



Replication of Status & Priority Tables

The ACS8514 is designed to partner an ACS8520 or ACS8530. As such there is a need to duplicate the input source quality information and input priorities. A similar need also arises in a redundant system where a slave system shadows a master system.

All devices can independently monitor their reference sources and determine the validity of each source. A facility to make it easier to share the input validity information is provided in the ACS8514, in the form of the *cnfg_sts_remote_sources_valid* register (registers 30 & 31). If one device reports an invalid channel, the same channel can be made invalid in another device by writing a zero to the relevant position in register 30 or 31.

Register *sts_sources_valid (*address 0E & 0F) reports a summary of the input status for each channel. This information can then be written to the *cnfg_sts_remote_sources_valid* register of the other device. This will ensure that any input source considered invalid by one device is also considered invalid by the other.

T4 Generation in Master and Slave ACS8514

As specified by the I.T.U., there is no need to align the phases of the T4 outputs in Master and Slave devices. For a fully redundant system, there is a need, however, to ensure that all devices select the same reference source. As there is no need to guarantee the alignment of phase of the T4 outputs, the Slave devices T4 input does not need to lock to the Masters T4 output, but only needs to ensure that it locks to the same external reference source. There is no defined Holdover requirement for the T4 path.

Output Clock Ports

The device supports outputs from the T4 DPLL in CMOS (TTL compatible) or AMI composite clock format.

TO1 is a CMOS direct digitally synthesized output from the T4 DPLL at E1/SDH (2.048 MHz) or DS1/SONET (1.544 MHz) rate. The output rate is set by register 64, bit 4. Since it is digitally derived it has an output jitter of typically 0.027 UI p-p at 2.048 MHz or 0.020 UI p-p at 1.544 MHz. This is 13 ns p-p and 3.8 ns RMS.

TO2 is an AMI format composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703[6]. Departures from the nominal pattern are detected within the ACS8514, and may cause reference-switching if too frequent. The jitter on the TO2 output is < 1ns p-p. See Table 29 for more output details.

The T4 outputs TO1 and TO2 can be enabled/disabled via register 63 bits [5:4].

Table 8 Output Table

Port Name	Output Port Technology	Frequencies Supported
TO1	TTL/CMOS	Fixed frequency, either 1.544 MHz or 2.048 MHz.
TO2	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz), fixed frequency.

Microprocessor Interface

Introduction to Microprocessor Modes

The ACS8514 incorporates a microprocessor interface, which can be configured for all common microprocessor interface types, via the bus interface mode control pins UPSEL(2:0) as defined in Table 9.

These pins are read at power up and set the interface mode.

The optional EPROM mode allows the internal registers to be loaded from the EPROM when the device comes out of "Power-On Reset" mode. The microprocessor interface type can be altered after power up by register 7F, such that for instance the device could boot up in EPROM mode and then switch to Motorola mode, for example, after the EPROM data has preconditioned the device. Reading of Data from the EPROM at boot up time is handled automatically by the ACS8514. The chip select of the EPROM should be driven from the micro in the case of mixed EPROM and micro communication, in order to avoid conflict between EPROM and ACS8514 access from the microprocessor.

The following sections show the interface timings for each interface type.

Table 9 Microprocessor Interface Mode Selection

UPSEL(2:0)	Mode	Description
111 (7)	OFF	Interface disabled
110 (6)	OFF	Interface disabled
101 (5)	SERIAL	Serial uP bus interface
100 (4)	MOTOROLA	Motorola interface
011 (3)	INTEL	Intel compatible bus interface
010 (2)	MULTIPLEXED	Multiplexed bus interface
001 (1)	EPROM	EPROM read mode
000 (0)	OFF	Interface disabled

Timing diagrams for the different microprocessor modes are presented in the following sections.

Motorola Mode

In MOTOROLA mode, the device is configured to interface with a microprocessor using a 680x0 type bus as parallel data + address. Figure 5 and Figure 6 show the timing diagrams of read and write accesses for this mode.

Figure 5 Read Access Timing in MOTOROLA Mode

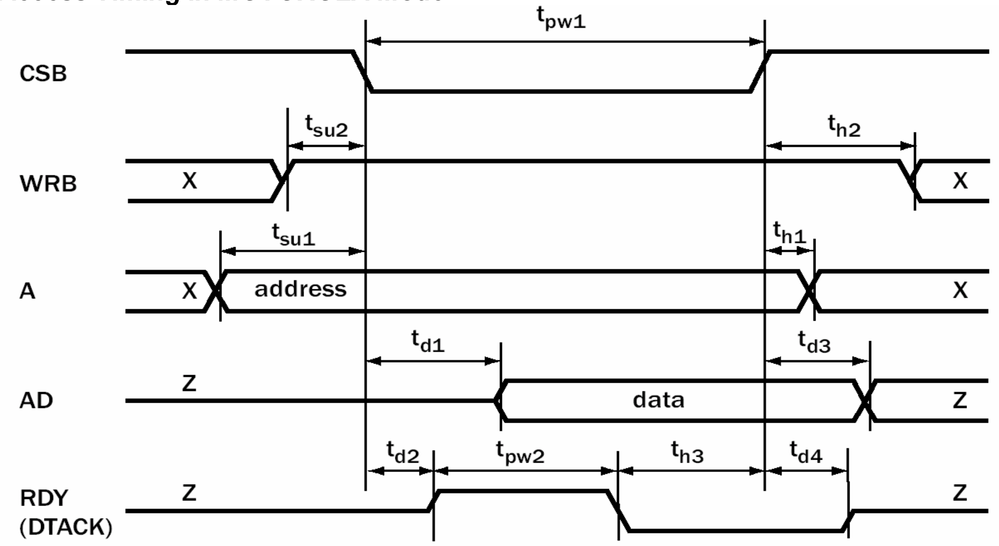


Table 10 Read Access Timing in MOTOROLA Mode (for use with Figure 5)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $CSB_{falling\ edge}$ to AD valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $CSB_{falling\ edge}$ to AD valid (consecutive Write - Read)	16 ns	-	192 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to $DTACK_{rising\ edge}$	-	-	13 ns
t_{d3}	Delay $CSB_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	CSB $_{Low\ time}$ (consecutive Read - Read)	25 ns	62 ns	-
	CSB $_{Low\ time}$ (consecutive Write - Read)	25 ns	193 ns	-
t_{pw2}	RDY $_{High\ time}$ (consecutive Read - Read)	12 ns	-	49 ns
	RDY $_{High\ time}$ (consecutive Write - Read)	12 ns	-	182 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold WRB valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB Low after $RDY_{falling\ edge}$	0 ns	-	-
t_p	Time between (consecutive Read - Read) accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	15 ns	-	-
t_p	Time between (consecutive Write - Read) accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Figure 6 Write Access Timing in MOTOROLA Mode

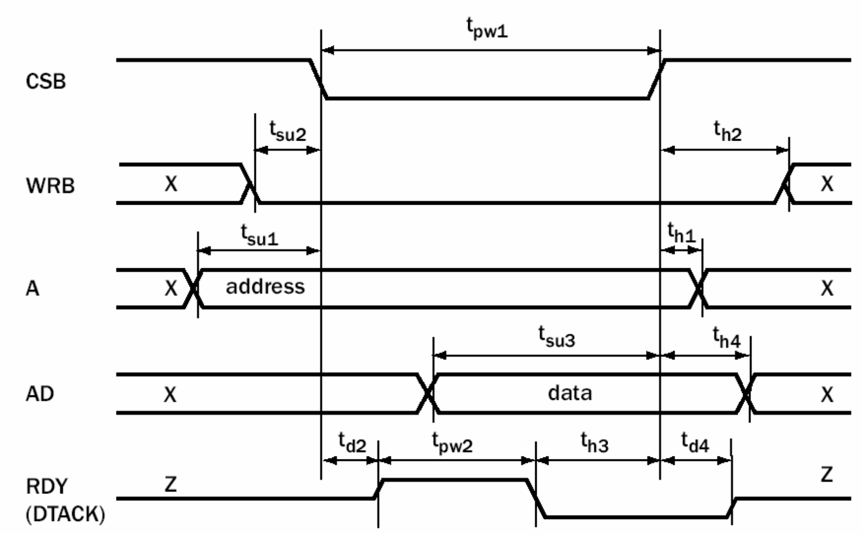


Table 11 Write Access Timing in MOTOROLA Mode (for use with Figure 6)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before $CSB_{rising\ edge}$	8 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to $RDY_{rising\ edge}$	-	-	13 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY High -Z	-	-	7 ns
t_{pw1}	$CSB_{Low\ time}$	25 ns	-	180 ns
t_{pw2}	$RDY_{High\ time}$	12 ns	-	166 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	8 ns	-	-
t_{h2}	Hold WRB Low after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB Low after $RDY_{falling\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after $CSB_{rising\ edge}$	9 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Intel Mode

In Intel mode, the device is configured to interface with a microprocessor using a 80x86 type bus as parallel data + address. Figure 7 and Figure 8 show the timing diagrams of read and write accesses for this mode.

Figure 7 Read Access Timing in INTEL Mode

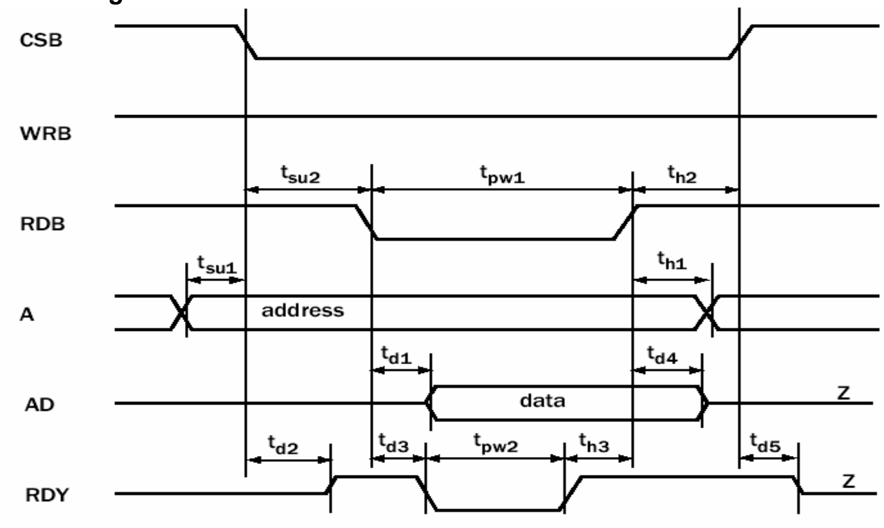


Table 12 Read Access Timing in INTEL Mode (for use with Figure 7)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $RDB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $RDB_{falling\ edge}$ to AD valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay $RDB_{falling\ edge}$ to AD valid (consecutive Write - Read)	12 ns	-	193 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $RDB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	14 ns
t_{d4}	Delay $RDB_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	11 ns
t_{pw1}	RDB Low time (consecutive Read - Read)	35 ns	60 ns	-
	RDB Low time (consecutive Write - Read)	35 ns	195 ns	-
t_{pw2}	RDY Low time (consecutive Read - Read)	20 ns	-	45 ns
	RDY Low time (consecutive Write - Read)	20 ns	-	182 ns
t_{h1}	Hold A valid after $RDB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold CSB Low after $RDB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB Low after $RDY_{rising\ edge}$	0 ns	-	-
t_p	Time between (consecutive Read - Read) accesses ($RDB_{rising\ edge}$ to $RDB_{falling\ edge}$, or $RDB_{rising\ edge}$ to $WRB_{falling\ edge}$)	15 ns	-	-
t_p	Time between (consecutive Write - Read) accesses (RDBrising edge to $RDB_{falling\ edge}$, or $RDB_{rising\ edge}$ to $WRB_{falling\ edge}$)	160 ns	-	-

Figure 8 Write Access Timing in INTEL Mode

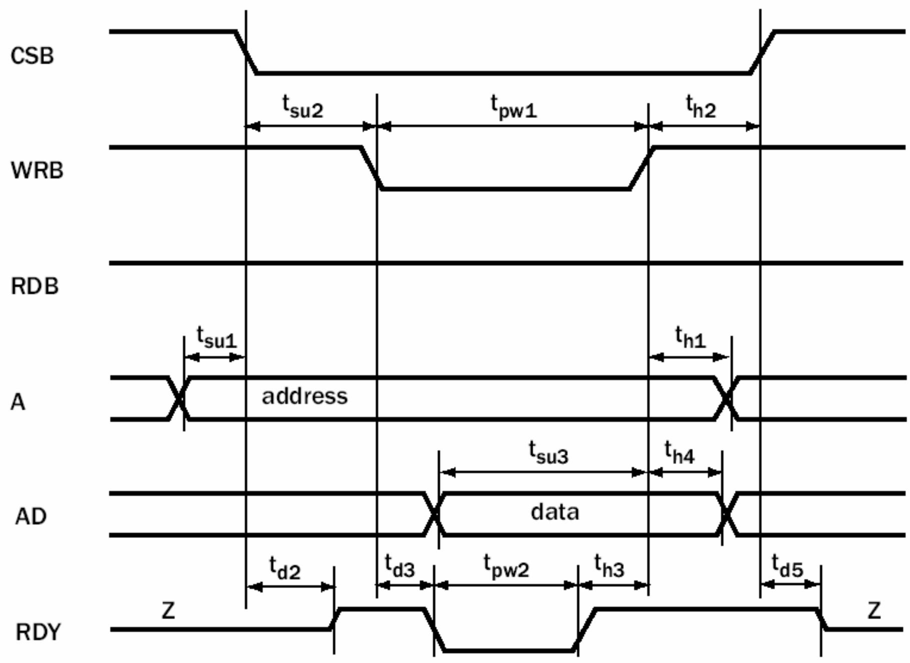


Table 13 Write Access Timing in INTEL Mode (for use with Figure 8)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to CSB$_{falling\ edge}$	4 ns	-	-
t_{su2}	Setup CSB$_{falling\ edge}$ to WRB$_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before WRB$_{rising\ edge}$	6 ns	-	-
t_{d2}	Delay CSB$_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay WRB$_{falling\ edge}$ to RDY$_{falling\ edge}$	-	-	14 ns
t_{d5}	Delay CSB$_{rising\ edge}$ to RDY high-Z	-	-	10 ns
t_{pw1}	WRB Low time	25 ns	185 ns	-
t_{pw2}	RDY Low time	10 ns	-	173 ns
t_{h1}	Hold A valid after WRB$_{rising\ edge}$	12 ns	-	-
t_{h2}	Hold CSB Low after WRB$_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB Low after RDY$_{rising\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after WRB$_{rising\ edge}$	4 ns	-	-
t_p	Time between consecutive accesses (WRB$_{rising\ edge}$ to WRB$_{falling\ edge}$, or WRB$_{rising\ edge}$ to RDB$_{falling\ edge}$)	160 ns	-	-

Multiplexed Mode

In Multiplexed Mode, the device is configured to interface with microprocessors (e.g., Intel's 80x86 family) which share bus signals between address and data. Figure 9 and Figure 10 show the timing diagrams of write and read accesses.

Figure 9 Read Access Timing in MULTIPLEXED Mode

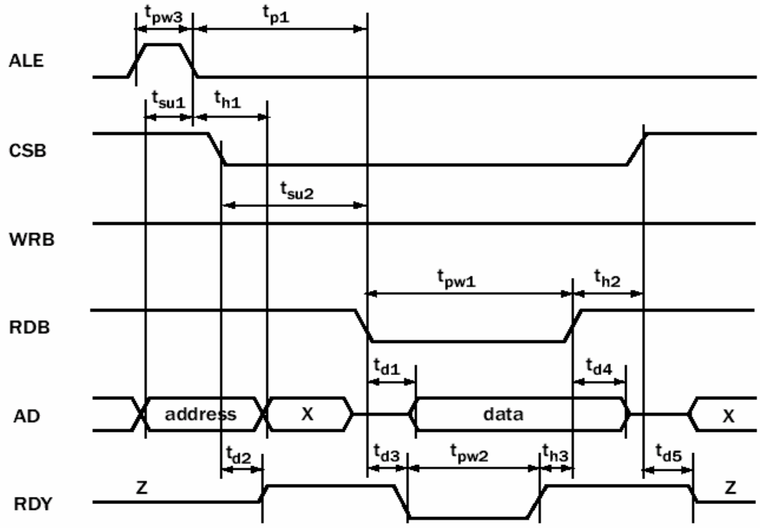


Table 14 Read Access Timing in MULTIPLEXED Mode (for use with Figure 9)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup AD address valid to ALE$_{\text{falling edge}}$	5 ns	-	-
t_{su2}	Setup CSB$_{\text{falling edge}}$ to RDB$_{\text{falling edge}}$	0 ns	-	-
t_{d1}	Delay RDB$_{\text{falling edge}}$ to AD data valid (consecutive Read - Read)	12 ns	-	40 ns
	Delay RDB$_{\text{falling edge}}$ to AD data valid (consecutive Write - Read)	17 ns	-	193 ns
t_{d2}	Delay CSB$_{\text{falling edge}}$ to RDY active	-	-	13 ns
t_{d3}	Delay RDB$_{\text{falling edge}}$ to RDYfalling edge	-	-	15 ns
t_{d4}	Delay RDB$_{\text{rising edge}}$ to AD data high-Z	-	-	10 ns
t_{d5}	Delay CSB$_{\text{rising edge}}$ to RDY high-Z	-	-	10 ns
t_{pw1}	RDB Low time (consecutive Read - Read)	35 ns	60 ns	-
	RDB Low time (consecutive Write - Read)	35 ns	200 ns	-
t_{pw2}	RDY Low time (consecutive Read - Read)	20 ns	-	40 ns
	RDY Low time (consecutive Write - Read)	20 ns	-	185 ns
t_{pw3}	ALE High time	5 ns	-	-
t_{h1}	Hold AD address valid after ALE$_{\text{falling edge}}$	9 ns	-	-
t_{h2}	Hold CSB Low after RDB$_{\text{rising edge}}$	0 ns	-	-
t_{h3}	Hold RDB Low after RDY$_{\text{rising edge}}$	0 ns	-	-
t_{p1}	Time between ALE$_{\text{falling edge}}$ and RDB$_{\text{falling edge}}$	0 ns	-	-
t_{p2}	Time between (consecutive Read - Read) accesses (RDB$_{\text{rising edge}}$ to ALE$_{\text{rising edge}}$)	20 ns	-	-
t_{p2}	Time between (consecutive Write - Read) accesses (RDB$_{\text{rising edge}}$ to ALE$_{\text{rising edge}}$)	160 ns	-	-

Figure 10 Write Access Timing in MULTIPLEXED Mode

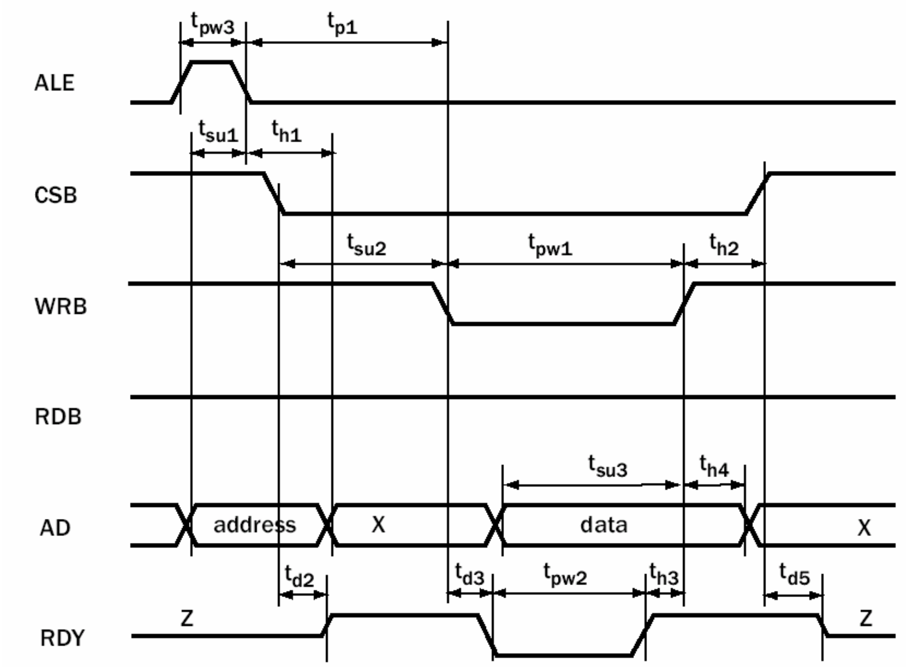


Table 15 Write Access Timing in MULTIPLEXED Mode (For use with Figure 10)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Set up AD address valid to $ALE_{falling\ edge}$	5 ns	-	-
t_{su2}	Set up $CSB_{falling\ edge}$ to $WRB_{falling\ edge}$	0 ns	-	-
t_{su3}	Set up AD data valid to $WRB_{rising\ edge}$	5 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $WRB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	15 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	WRB Low time	30 ns	188 ns	-
t_{pw2}	RDY Low time	15 ns	-	173 ns
t_{pw3}	ALE High time	5 ns	-	-
t_{h1}	Hold AD address valid after $ALE_{falling\ edge}$	9 ns	-	-
t_{h2}	Hold CSB Low after $WRB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB Low after $RDY_{rising\ edge}$	0 ns	-	-
t_{h4}	AD data hold valid after $WRB_{rising\ edge}$	7 ns	-	-
t_{p1}	Time between $ALE_{falling\ edge}$ and $WRB_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between consecutive accesses ($WRB_{rising\ edge}$ to $ALE_{rising\ edge}$)	1600 ns	-	-

Serial Mode

In SERIAL Mode, the device is configured to interface with a serial microprocessor bus. Figure 11 and Figure 12 show the timing diagrams of write and read accesses for this mode. The serial interface can be SPI compatible.

The Motorola SPI convention is such that address and data is transmitted and received MSB first. On the ACS8514, device address and data are transmitted and received LSB first. Address, read/write control and data on the SDI pin is latched into the device on the rising edge of the SCLK. During a read operation, serial data output on the SDO pin can be read out of the device on either the rising or falling edge of the SCLK depending on the logic level of CLKE. For standard Motorola SPI compliance, data should be clocked out of the SDO pin on the rising edge of the SCLK so that it may be latched into the microprocessor on the falling edge of the SCLK.

The serial interface clock (SCLK) is not required to run between accesses (i.e., when CSB = 1).

Figure 11 Read Access Timing in SERIAL Mode

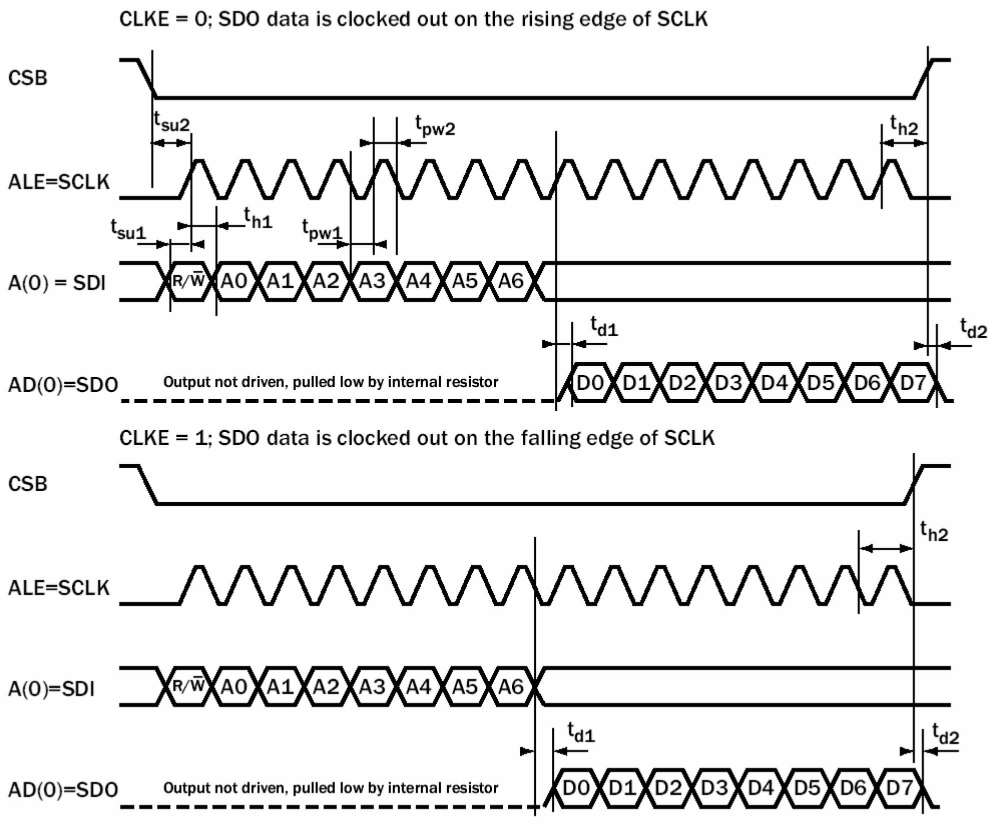


Table 16 Read Access Timing in SERIAL Mode (For use with Figure 11)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	14 ns	-	-
t_{d1}	Delay $SCLK_{rising\ edge}$ ($SCLK_{falling\ edge}$ for CLKE = 1) to SDO valid	-	-	18 ns
t_{d2}	Delay $CSB_{rising\ edge}$ to SDO high-Z	-	-	16 ns

Table 16 Read Access Timing in SERIAL Mode (For use with Figure 11) (continued)

Symbol	Parameter	MIN	TYP	MAX
t_{pw1}	SCLK Low time	22 ns	-	-
t_{pw2}	SCLK High time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB Low after $SCLK_{rising\ edge}$, for CLKE = 0 Hold CSB Low after $SCLK_{falling\ edge}$, for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

Figure 12 Write Access Timing in SERIAL Mode

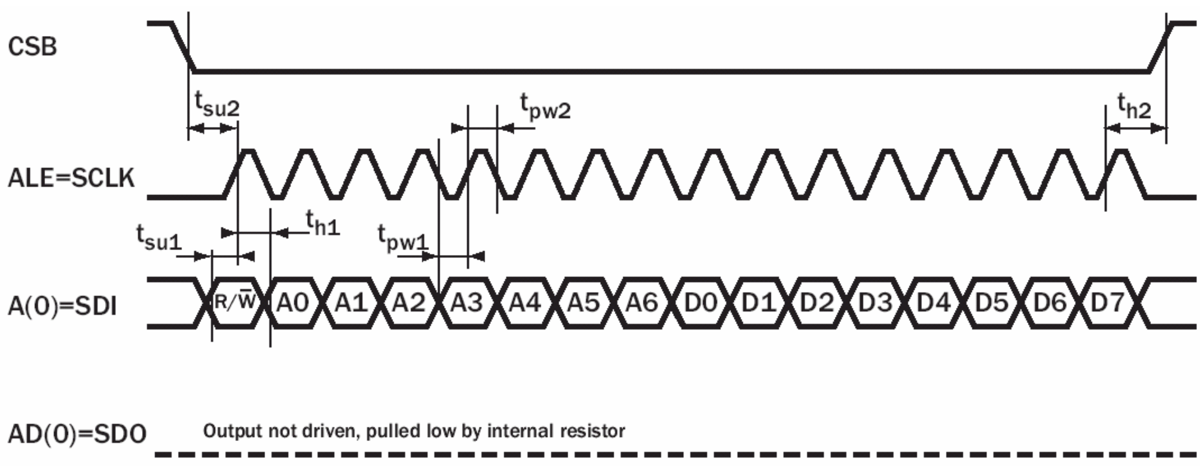


Table 17 Write Access Timing in SERIAL Mode (For use with Figure 12)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	14 ns	-	-
t_{pw1}	SCLK Low time	22 ns	-	-
t_{pw2}	SCLK High time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB Low after $SCLK_{rising\ edge}$	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

EPROM Mode

This mode is suitable for use with an EPROM, in which configuration data is stored (one-way communication - status information will not be accessible). A state machine internal to the ACS8514 device will perform numerous EPROM read operations to read the data out of the EPROM. In EPROM Mode, the ACS8514 takes control of the bus as Master and reads the device set-up from an AMD AM27C64 type EPROM at lowest speed (250ns) after device set-up (system reset). The EPROM access state machine in the up interface sequences the accesses. Figure 13 shows the access timing of the device in EPROM mode.

Further information can be found in the AMD AM27C64 data sheet.

Figure 13 Access Timing in EPROM mode

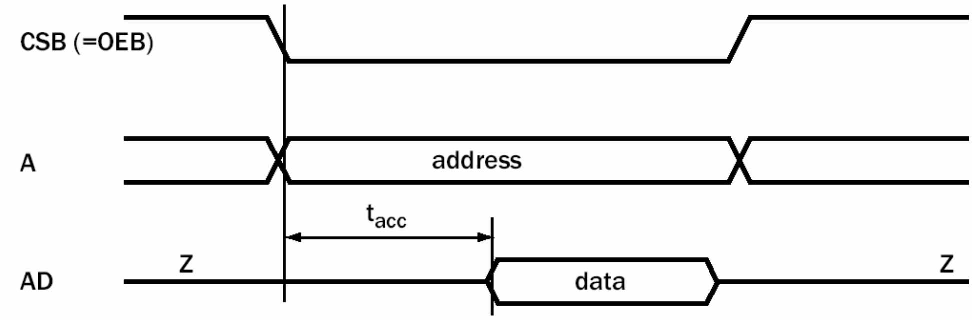


Table 18 Access Timing in EPROM mode (For use with Figure 13)

Symbol	Parameter	MIN	TYP	MAX
t_{acc}	Delay $CSB_{falling\ edge}$ or A change to AD valid	-	-	920 ns

Power-On Reset

The Power-On Reset (PORB) pin resets the device if forced Low. The reset is asynchronous; the minimum Low pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Reset must be asserted at power on, and may be re-asserted at any time to restore defaults. This is implemented simply using an external capacitor to GND along with the internal pull-up resistor. The ACS8514 is held in a reset state for 250 ms after the PORB pin has been pulled high. In normal operation PORB should be held high.

Register Map

Each Register, or register group, is described in the following Register Map and subsequent Register Description Tables.

Register Organization

The ACS8514 SETS uses a total of 104 8-bit registers, identified by a Register Name and corresponding hexadecimal Register Address. They are presented here in ascending order of Reg. address and each Register is organized with the most-significant bit positioned in the left-most bit, and bit significance decreasing towards the right-most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g. flags) upwards. Several data fields are spread across multiple registers, as shown in the Register Map. Shaded areas in the map are "don't care" and writing either 0 or 1 will not affect any function of the device. Bits labeled "Set to zero" or "Set to one" must be set as stated during initialization of the device, either following power- up, or after a Power-On Reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

CAUTION! Do not write to any undefined register addresses as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Multi-word Registers

For Multi-word Registers (e.g. register 0C & 0D), all the words have to be written to their separate addresses, and without any other access taking place, before their combined value can take effect. If the sequence is interrupted, the sequence of writes will be ignored. Reading a multi-word address freezes the other address words of a multi-word address so that the bytes all correspond to the same complete word.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the *chip_id* register (addr. 00) and *chip_revision* registers (addr. 02). Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the *sts_interrupts* register), any individual data field may be cleared by writing a 1 into each bit of the field (writing a 0 value into a bit will not affect the value of the bit). A description of each register is given in the Register Map, and Register Map Description.

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pin-settable. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writeable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ; the active state (High or Low) is programmable and the pin can either be driven, or set to high impedance when non-active (Reg 7D refers). Bits in the interrupt status register are set (High) by the following conditions;

1. Any reference source becoming valid or going invalid.
2. A change in the operating state (e.g. Locked, Holdover etc.)
3. A brief loss of the currently selected reference source.
4. An AMI input error.

All interrupt sources (see register 05, 06 & 08) are maskable via the mask register, each one being enabled by writing a 1 to the appropriate bit. Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted. All interrupts are cleared by writing a 1 to the bit(s) to be cleared in the status register. When all pending unmasked interrupts are cleared the interrupt pin will go inactive.

Defaults

Each Register is given a defined default value at reset and these are listed in the Map and Description Tables. However, some read-only status registers may not necessarily show the same default values after reset as those given in the tables. This is because they reflect the status of the device which may have changed in the time it takes to carry out the read, or through reasons of configuration. In the same way, the default values given for shaded areas could also take different values to those stated.

Table 19 Register Map

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit							
			7 (MSB)	*6*	*5*	*4*	*3*	*2*	*1*	*0 (LSB)*
chip_id (RO)	*00*	*52*	Device part number [7:0] 8 least significant bits of the chip ID							
	01	*21*	Device part number [15:8] 8 most significant bits of the chip ID							
chip_revision (RO)	*02*	*00*	Chip revision number [7:0]							
test_register1. (R/W)	*03*	*14*	phase_ alarm	disable_180			Set to zero	8k Edge Polarity	Set to zero	Set to zero
sts_interrupts. (R/W)	*05*	*FF*	I8 valid change	I7 valid change	I6 valid change	I5 valid change	I4 valid change	I3 valid change	I2 valid change	I1 valid change
	06	*3F*	MonDPLL_ state	Mon_ref_ failed	I14 valid change	I13 valid change	I12 valid change	I11 valid change	I10 valid change	I9 valid change
sts_current_DPLL_frequency., OC/OD	*07*	*00*						sts_current_DPLL_frequency[18:16]		
sts_interrupts. (R/W)	*08*	*50*		T4_status		T4_inputs_ failed	AMI2_Viol	AMI2_LOS	AMI1_Viol	AMI1_LOS
sts_operating. (RO)	*09*	*41*		T4_DPLL_Lock	Mon_DPLL_freq_soft_alarm	T4_DPLL_ freq_ soft_alarm				
sts_priority_table. (RO)	*0A*	*00*	Highest priority validated source				Currently selected source			
	0B	*00*					2 nd highest priority validated source			
sts_current_DPLL_frequency. (RO)	*0C*	*00*	Bits [7:0] of current DPLL frequency							
	0D	*00*	Bits [15:8] of current DPLL frequency							
	07	*00*						Bits [18:16] of current DPLL frequency		
sts_sources_valid. (RO)	*0E*	*00*	I8	I7	I6	I5	I4	I3	I2	I1
	0F	*00*			I14	I13	I12	I11	I10	I9
sts_reference_sources. (RO) *Status of inputs:*			Out-of-band alarm (soft)	Out-of-band alarm (hard)	No activity alarm	Phase lock alarm	Out-of-band alarm (soft)	Out of band alarm (hard)	No activity alarm	Phase lock alarm
(1 & 2).	*10*	*66*	Status of I2 Input				Status of I1 Input			
(3 & 4).	*11*	*66*	Status of I4 Input				Status of I3 Input			
(5 & 6).	*12*	*66*	Status of I6 Input				Status of I5 Input			
(7 & 8).	*13*	*66*	Status of I8 Input				Status of I7 Input			
(9 & 10).	*14*	*66*	Status of I10 Input				Status of I9 Input			
(11 & 12).	*15*	*66*	Status of I12 Input				Status of I11 Input			
(13 & 14).	*16*	*66*	Status of I14 Input				Status of I13 Input			
cnfg_ref_selection_priority (1 & 2).	*18*	*32*	programmed_priority I2				programmed_priority I1			
(R/W) (3 & 4).	*19*	*54*	programmed_priority I4				programmed_priority I3			
(5 & 6).	*1A*	*76*	programmed_priority I6				programmed_priority I5			
(7 & 8).	*1B*	*98*	programmed_priority I8				programmed_priority I7			
(9 & 10).	*1C*	*BA*	programmed_priority I10				programmed_priority I9			
(11 & 12).	*1D*	*DC*	programmed_priority I12				programmed_priority I11			
(13 & 14).	*1E*	*FE*	programmed_priority I14				programmed_priority I13			
cnfg_ref_source_frequency(R/W) 1.	*20*	*00*	Set to zero		bucket_id_1		Set to zero			
2.	*21*	*00*	Set to zero		bucket_id_2		Set to zero			
3.	*22*	*00*	divn_3	lock8k_3	bucket_id_3		reference_source_frequency_3			
4.	*23*	*00*	divn_4	lock8k_4	bucket_id_4		reference_source_frequency_4			
5.	*24*	*03*	divn_5	lock8k_5	bucket_id_5		reference_source_frequency_5			
6.	*25*	*03*	divn_6	lock8k_6	bucket_id_6		reference_source_frequency_6			
7.	*26*	*03*	divn_7	lock8k_7	bucket_id_7		reference_source_frequency_7			
8.	*27*	*03*	divn_8	lock8k_8	bucket_id_8		reference_source_frequency_8			
9.	*28*	*03*	divn_9	lock8k_9	bucket_id_9		reference_source_frequency_9			
10.	*29*	*03*	divn_10	lock8k_10	bucket_id_10		reference_source_frequency_10			
11.	*2A*	*03*	divn_11	lock8k_11	bucket_id_11		reference_source_frequency_11			
12.	*2B*	*01*	divn_12	lock8k_12	bucket_id_12		reference_source_frequency_12			
13.	*2C*	*01*	divn_13	lock8k_13	bucket_id_13		reference_source_frequency_13			
14.	*2D*	*01*	divn_14	lock8k_14	bucket_id_14		reference_source_frequency_14			
cnfg_sts_remote_sources_valid. (R/W)	*30*	*FF*	Remote status, channels <8:1>							
	31	*3F*			Remote status, channels <14:9>					
force_select_reference_source. (R/W)	*33*	*0F*					Mon_DPLL_ref_source			
cnfg_input_mode. (R/W)	*34*	*C2*	Set to 0	Set to 1	Set to 0	Set to 0	Set to 0	ip_sonsdhb		Set to 1
cnfg_T4_path. (R/W)	*35*	*40*	Set to 0	T4_dig_feed-back		Set to 0	T4_forced_reference_source			
cnfg_differential_inputs. (R/W)	*36*	*02*							I6_PECL	I5_LVDS
cnfg_uPsel_pins. (RO)	*37*	*02*						Microprocessor type		
cnfg_auto_bw_sel. (R/W)	*3B*	*FB*	Set to 0				Mon_lim_int			
cnfg_nominal_frequency(R/W)[7:0].	*3C*	*99*	Nominal frequency [7:0]							
[15:8].	*3D*	*99*	Nominal frequency [15:8]							
cnfg_average_frequency. [7:0]	*3E*	*00*	average_frequency[7:0]							
(R/W) [15:8]	*3F*	*00*	average_frequency_value[15:8]							

Register Name RO = Read Only *R/W = Read/Write*	Address (hex)	Default (hex)	Data Bit *7 (MSB)*	6	5	4	3	2	1	*0 (LSB)*
cnfg_averager_modes. (R/W)	*40*	*88*	freq_ averaging	fast_averaging	Set to 1	Set to 0	Set to 1	average_frequency_value*[18:16]* (with Registers 3E and 3F above)		
cnfg_DPLL_freq_limit. (R/W [7:0]	*41*	*76*	DPLL_freq_limit_value[7:0]							
[9:8]	*42*	*00*							DPLL_freq_limit_value[9:8]	
cnfg_interrupt_mask. (R/W) [7:0]	*43*	*00*	I8 interrupt not masked	I7 interrupt not masked	I6 interrupt not masked	I5 interrupt not masked	I4 interrupt not masked	I3 interrupt not masked	I2 interrupt not masked	I1 interrupt not masked
[15:8]	*44*	*00*	MonDPLL_ state	Mon_ref_failed	I14 interrupt not masked	I13 interrupt not masked	I12 interrupt not masked	I11 interrupt not masked	I10 interrupt not masked	I9 interrupt not masked
[23:16]	*45*	*00*	Set to 0	T4_status		T4_inputs_ failed	AMI2_Viol	AMI2_LOS	AMI1_Viol	AMI1_LOS
cnfg_freq_divn. (R/W) [7:0]	*46*	*FF*	divn_value [7:0]							
[13:8]	*47*	*3F*			divn_value [13:8]					
cnfg_monitors. (R/W)	*48*	*05*	Set to 1	los_flag_on_ TDO	Set to 0	Set to 0	Set to 0	Set to 0	freq_monitor_ soft_enable	freq_monitor_ hard_enable
cnfg_freq_mon_threshold. (R/W)	*49*	*23*	soft_frequency_alarm_threshold [3:0]				hard_frequency_alarm_threshold [3:0]			
cnfg_current_freq_mon_threshold. (R/W)	*4A*	*23*	current_soft_frequency_alarm_threshold [3:0]				current_hard_frequency_alarm_threshold [3:0]			
cnfg_registers_source_select (R/W)	*4B*	*00*				T4orMon_s elect	frequency_measurement_channel_select			
sts_freq_measurement. (R/W)	*4C*	*00*	freq_measurement_value [7:0]							
cnfg_DPLL_soft_limit. (R/W)	*4D*	*8E*	freq_lim_ ph_loss	DPLL_soft_limit_value[6:0] Resolution = 0.628 ppm						
cnfg_upper_threshold_0. (R/W)	*50*	*06*	Configuration 0: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_0. (R/W)	*51*	*04*	Configuration 0: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_0. (R/W)	*52*	*08*	Configuration 0: Activity alarm bucket size [7:0]							
cnfg_decay_rate_0. (R/W)	*53*	*01*							Cfg 0:decay_rate [1:0]	
cnfg_upper_threshold_1. (R/W)	*54*	*06*	Configuration 1: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_1. (R/W)	*55*	*04*	Configuration 1: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_1. (R/W)	*56*	*08*	Configuration 1: Activity alarm bucket size [7:0]							
cnfg_decay_rate_1. (R/W)	*57*	*01*							Cfg 1:decay_rate [1:0]	
cnfg_upper_threshold_2. (R/W)	*58*	*06*	Configuration 2: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_2. (R/W)	*59*	*04*	Configuration 2: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_2. (R/W)	*5A*	*08*	Configuration 2: Activity alarm bucket size [7:0]							
cnfg_decay_rate_2. (R/W)	*5B*	*01*							Cfg 2:decay_rate [1:0]	
cnfg_upper_threshold_3. (R/W)	*5C*	*06*	Configuration 3: Activity alarm set threshold [7:0]							
cnfg_lower_threshold_3. (R/W)	*5D*	*04*	Configuration 3: Activity alarm reset threshold [7:0]							
cnfg_bucket_size_3. (R/W)	*5E*	*08*	Configuration 3: Activity alarm bucket size [7:0]							
cnfg_decay_rate_3. (R/W)	*5F*	*01*							Cfg 3:decay_rate [1:0]	
	60	*85*	Set all bits to 0							
	61	*86*								
	62	*8A*								
cnfg_output_enab	*63*	*F6*	Set to 0	Set to 0	TO1_en	TO2_en	Set to 0	Set to 0	Set to 0	Set to 0
cnfg_T4_DPLL_frequency. (R/W)	*64*	*01*		Auto_squelch_ T4	AMI_op_duty	T4_op_ SONSDH		T4_DPLL_Enable		
cnfg_T4_meas_phase (R/W)	*65*	*01*	T4_meas_ phas	Set to 0				Set to 0	Set to 0	Set to 1
cnfg_T4_DPLL_bw. (R/W)	*66*	*00*							T4_DPLL_bandwidth *[1:0]*	
cnfg_Mon_DPLL_bw (R/W)	*67*	*0B*					Monitor_DPLL_bandwidth			
cnfg_T4_DPLL_damping. (R/W)	*6A*	*13*		Set to 0	Set to 0	Set to 1		T4_damping		
cnfg_Mon_DPLL_damping. (R/W)	*6B*	*13*		Set to 0	Set to 0	Set to 1		Mon_DPLL_damping		
cnfg_phase_loss_fine_limit (R/W)	*73*	*A2*	Fine limit Phase loss enable	No activity for phase loss	Test bit Set to 1			phase_loss_fine_limit [2:0]		
cnfg_phase_loss_coarse_limit. (R/W)	*74*	*85*	Coarse limit Phase loss enable	Wide range enable	Enable Multi Phase resp.		Phase loss coarse limit in UI pk-pk [3:0]			
cnfg_phasemon. (R/W)	*76*	*06*	Input noise window enable							
sts_current_phase. (RO) *[7:0].*	*77*	*00*	current_phase[7:0]							
[15:8].	*78*	*00*	current_phase[15:8]							
cnfg_interrupt. (R/W)	*7D*	*02*						GPO interrupt enable	Interrupt tristate enable	Interrupt polarity enable
cnfg_protection.(R/W)	*7E*	*85*	protection_value							
cnfg_uPsel. (R/W)	*7F*	*02**						Microprocessor type (*Default value depends on value on UPSEL[2:0] pins)		

Register Descriptions

Address(hex): 00

Register Name	*chip_id*		**Description**	(RO) 8 least significant bits of the chip ID.		**Default Value**	0101 0010
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
chip_id[7:0]							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*chip_id* Least significant byte of the 2-byte device ID	52 (hex)	2152 hex = 8530 decimal = chip type 8530 is indicated since this is the internal die type used, even though it is packaged as ACS8514

Address(hex): 01

Register Name	*chip_id*		**Description**	(RO) 8 most significant bits of the chip ID.		**Default Value**	0010 0001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
chip_id[15:8]							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*chip_id* Most significant byte of the 2-byte device ID	21 (hex)	2152 hex = 8530 decimal = chip type See register 00 description

Address(hex): 02

Register Name	*chip_revision*		**Description**	(RO) Silicon revision of the device.		**Default Value**	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
chip_revision[7:0]							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*chip_revision* Silicon revision of the device	00 (hex)	Version revision

Address(hex): 03

Register Name	*test_register1*		**Description**	(R/W) Register containing various test controls (not normally used).		**Default Value**	0001 0100
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
phase_alarm	*disable_180*			*Set to zero*	*8k Edge Polarity*	*Set to zero*	*Set to zero*

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*phase_alarm* (phase alarm (R/O)) Instantaneous result from Monitor DPLL	0 1	Monitor DPLL reporting phase locked. Monitor DPLL reporting phase lost.

Address(hex): 03 (continued)

Bit No.	Description	Bit Value	Value Description
6	*disable_180* Normally the DPLLs will try to lock to the nearest edge (±180°) for the first 2 seconds when locking to a new reference. If the DPLL does not determine that it is phase locked after this time, then the capture range reverts to ±360°, which corresponds to frequency and phase locking. Forcing the DPLL into frequency locking mode may reduce the time to frequency lock to a new reference by up to 2 seconds. However, this may cause an unnecessary phase shift of up to 360° when the new and old references are very close in frequency and phase.	0 1	Monitor DPLL automatically determines frequency lock enable. Monitor DPLL forced to always frequency and phase lock.
5, 4	Not used.	-	-
2	*8k Edge Polarity* When lock 8k mode is selected for the current input reference source, this bit allows the system to lock on either the rising or the falling edge of the input clock.	0 1	Lock to falling clock edge. Lock to rising clock edge.
3,1,0	Test Control Leave unchanged or set to zero	0	-

Address(hex): 05

Register Name	*sts_interrupts*		Description	(R/W) Bits [7:0] of the interrupt status register.		Default Value	1111 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* Interrupt indicating that input I8 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I8 has not changed status (valid/invalid). Input I8 has changed status (valid/invalid). Writing 1 resets the input to 0.
6	*I7* Interrupt indicating that input I7 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I7 has not changed status (valid/invalid). Input I7 has changed status (valid/invalid). Writing 1 resets the input to 0.
5	*I6* Interrupt indicating that input I6 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I6 has not changed status (valid/invalid). Input I6 has changed status (valid/invalid). Writing 1 resets the input to 0.
4	*I5* Interrupt indicating that input I5 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I5 has not changed status (valid/invalid). Input I5 has changed status (valid/invalid). Writing 1 resets the input to 0.
3	*I4* Interrupt indicating that input I4 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I4 has not changed status (valid/invalid). Input I4 has changed status (valid/invalid). Writing 1 resets the input to 0.

Address(hex): 05 (continued)

Bit No.	Description	Bit Value	Value Description
2	*I3* Interrupt indicating that input I3 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I3 has not changed status (valid/invalid). Input I3 has changed status (valid/invalid). Writing 1 resets the input to 0.
1	*I2* Interrupt indicating that input I2 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I2 has not changed status (valid/invalid). Input I2 has changed status (valid/invalid). Writing 1 resets the input to 0.
0	*I1* Interrupt indicating that input I1 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I1 has not changed status (valid/invalid). Input I1 has changed status (valid/invalid). Writing 1 resets the input to 0.

Address(hex): 06

Register Name	*sts_interrupts*		**Description**	(R/W) bits [15:8] of the interrupt status register.		**Default Value**	0011 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
MonDPLL_state	*Mon_ref_failed*	*I14*	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
7	*MonDPLL_state* Interrupt indicating that the lock state of the Monitor DPLL has changed. Latched until reset by software writing a 1 to this bit.	0 1	Operating mode has not changed. Operating mode has changed. Writing 1 resets the input to 0.
6	*Mon_ref_failed* Interrupt indicating that input to the Monitor DPLL has failed. This interrupt will be raised after 2 missing input cycles. This is much quicker than waiting for the input to become invalid. This input is not generated in Free-run or Holdover modes. Latched until reset by software writing a 1 to this bit.	0 1	Input to the Monitor DPLL is valid. Input to the Monitor DPLL has failed. Writing 1 resets the input to 0.
5	*I14* Interrupt indicating that input I14 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I14 has not changed status (valid/invalid). Input I14 has changed status (valid/invalid). Writing 1 resets the input to 0.
4	*I13* Interrupt indicating that input I13 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I13 has not changed status (valid/invalid). Input I13 has changed status (valid/invalid). Writing 1 resets the input to 0.
3	*I12* Interrupt indicating that input I12 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I12 has not changed status (valid/invalid). Input I12 has changed status (valid/invalid). Writing 1 resets the input to 0.
2	*I11* Interrupt indicating that input I11 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I11 has not changed status (valid/invalid). Input I11 has changed status (valid/invalid). Writing 1 resets the input to 0.

Address(hex): 06 (continued)

Bit No.	Description	Bit Value	Value Description
1	*I10* Interrupt indicating that input I10 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I10 has not changed status (valid/invalid). Input I10 has changed status (valid/invalid). Writing 1 resets the input to 0.
0	*I9* Interrupt indicating that input I9 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input I9 has not changed status (valid/invalid). Input I9 has changed status (valid/invalid). Writing 1 resets the input to 0.

Address(hex): 07

Register Name	*sts_current_DPLL_frequency [18:16]*		Description	(RO) Bits [18:16] of the current DPLL frequency.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					sts_current_DPLL_frequency[18:16]		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	*sts_current_DPLL_frequency[18:16]* When bit 4 of register 4B = 0 the frequency for the monitor path is reported. When this Bit 4 = 1 the frequency for the T4 path is reported.	-	See register description of sts_current_DPLL_frequency. at address 0D hex.

Address(hex): 08

Register Name	*sts_interrupts*		Description	(R/W) Bits [23:16] of the interrupt status register.		Default Value	0101 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	T4_status		*T4_inputs_ failed*	*AMI2_Viol*	*AMI2_LOS*	*AMI1_Viol*	*AMI1_LOS*

Bit No.	Description	Bit Value	Value Description
7, 5	Not used	-	-
6	*T4_status* Interrupt indicating that the T4 DPLL has lost lock (if it was locked) or gained lock (if it was not locked). Latched until reset by software writing a 1 to this bit.	0 1	Input to the T4 DPLL has not changed. Input to the T4 DPLL has lost/gained lock. Writing 1 resets the input to 0.
4	*T4_inputs_failed* Interrupt indicating that no valid inputs are available to the T4 DPLL. Latched until reset by software writing a 1 to this bit.	0 1	T4 DPLL has valid inputs. T4 DPLL has no valid inputs. Writing 1 resets the input to 0.
3	*AMI2_Viol* Interrupt indicating that an AMI Violation error has occurred on input I2. Latched until reset by software writing a 1 to this bit.	0 1	Input I2 has had no violation error. Input I2 has had a violation error. Writing 1 resets the input to 0.

Address(hex): 08 (continued)

Bit No.	Description	Bit Value	Value Description
2	*AMI2_LOS* Interrupt indicating that an AMI LOS error has occurred on input I2. Latched until reset by software writing a 1 to this bit.	0 1	Input I2 has had no LOS error. Input I2 has had a LOS error. Writing 1 resets the input to 0.
1	*AMI1_Viol* Interrupt indicating that an AMI Violation error has occurred on input I1. Latched until reset by software writing a 1 to this bit.	0 1	Input I1 has had no violation error. Input I1 has had a violation error. Writing 1 resets the input to 0.
0	*AMI1_LOS* Interrupt indicating that an AMI LOS error has occurred on input I1. Latched until reset by software writing a 1 to this bit.	0 1	Input I1 has had no LOS error. Input I1 has had a LOS error. Writing 1 resets the input to 0.

Address(hex): 09

Register Name	*sts_operating*		Description	(RO) Current operating state of the internal DPLL's.		Default Value	0100 0001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	T4_DPLL_Lock	*Mon_DPLL_freq_soft_alarm*	*T4_DPLL_freq_soft_alarm*				

Bit No.	Description	Bit Value	Value Description
7, 3, 2, 1, 0	Not used	-	-
6	*T4_DPLL_Lock* The bit indicates that the T4 DPLL is locked by monitoring the T4DPLL phase loss indicators, which potentially come from four sources. The four phase loss indicators are enabled by the same registers that enable them for the Monitor DPLL, as follows: the fine phase loss detector enabled by register 73 bit 7, the coarse phase loss detector enabled by register 74 bit 7, the phase loss indication from no activity on the input enabled by register 73 bit 6 and phase loss from the DPLL being at its min or max frequency limits enabled by register 4D bit 7. For this T4_DPLL_lock indication this bit will latch an indication of phase lost from the coarse phase lock detector such that when an indication of phase lost (or not locked) is set it stays in that phase lost or not locked state (so this bit = 0). Since this bit latches the indication of phase lost from the coarse phase loss detector, then for this bit to give a correct current reading of the T4 DPLL locked state, then the coarse phase loss detector should be temporarily disabled (register 74, bit 7 = 0), then the T4_DPLL_lock bit can be read, then the coarse phase loss detector should be re-enabled again (register 74, bit7=1).	0 1	T4 DPLL not phase locked to reference source. T4 DPLL phase locked to reference source. Once this bit is indicating 'locked' (=1), it is always a correct indication and no change to the coarse phase loss detector enable is required. If at any time any cycle slips occur that trigger the coarse phase loss detector (which monitors cycle slips) then this information is latched so that the lock bit (reg 09, bit 6) will go low and stay low, indicating that a problem has occurred. It is then a requirement that the coarse phase loss detector disable / re-enable sequence is performed during a read of the T4 locked bit, in order to get a current indication of whether the T4 DPLL is locked. It is recommended that register 73 bit 6 is set to '1' so that no activity on the input sets phase lost and hence sets *T4_DPLL_Lock* = 0 , otherwise a locked indication can be indicated in the case of no input clock, since all other phase loss indicators are in a holding state. Register 73, bit 6 = 1 avoids this case and gives correct lock indication.

Address(hex): 09 (continued)

Bit No.	Description	Bit Value	Value Description
5	*Monitor_DPLL_freq_soft_alarm* The Monitor DPLL has a programmable "soft" alarm frequency limit. This is an alarm raised that does not cause a disqualification of the input. This bit reports the status of the "soft" alarm.	0 1	Monitor DPLL tracking its reference within the limits of the programmed "soft" alarm. Monitor DPLL tracking its reference beyond the limits of the programmed "soft" alarm.
4	*T4_DPLL_freq_soft_alarm* The T4 DPLL has a programmable "soft" alarm frequency limit. This is an alarm raised that does not cause a disqualification of the input. This bit reports the status of the "soft" alarm.	0 1	T4 DPLL tracking its reference within the limits of the programmed "soft" alarm. T4 DPLL tracking its reference beyond the limits of the programmed "soft" alarm.

Address(hex): 0A

Register Name	*sts_priority_table*		**Description**	(RO) Bits [7:0] of the validated priority table.		**Default Value**	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Highest priority validated source				*Currently selected source*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*Highest priority validated source* Reports the input channel number of the highest priority validated source. Note that if an input is valid and it does not appear in this field, then the input may have been disallowed in register 30, 31h. Register 4B, bit 4 must be set to ‘1’ for correct setting and reporting of the T4 DPLL priorities.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	No valid source available. Input I1 is the highest priority valid source. Input I2 is the highest priority valid source. Input I3 is the highest priority valid source. Input I4 is the highest priority valid source. Input I5 is the highest priority valid source. Input I6 is the highest priority valid source. Input I7 is the highest priority valid source. Input I8 is the highest priority valid source. Input I9 is the highest priority valid source. Input I10 is the highest priority valid source. Input I11 is the highest priority valid source. Input I12 is the highest priority valid source. Input I13 is the highest priority valid source. Input I14 is the highest priority valid source. Not used.
[3:0]	*Currently selected source* Reports the input channel number of the currently selected source. When in Non-revertive mode, this is not necessarily the same as the highest priority validated source. Note that if an input is valid and it does not appear in this field, then the input may have been disallowed in register 30, 31h. This value will be the same as the highest priority validated source. Register 4B, bit 4 must be set to ‘1’ for correct setting and reporting of the T4 DPLL priorities.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	No source currently selected. Input I1 is the currently selected source. Input I2 is the currently selected source. Input I3 is the currently selected source. Input I4 is the currently selected source. Input I5 is the currently selected source. Input I6 is the currently selected source. Input I7 is the currently selected source. Input I8 is the currently selected source. Input I9 is the currently selected source. Input I10 is the currently selected source. Input I11 is the currently selected source. Input I12 is the currently selected source. Input I13 is the currently selected source. Input I14 is the currently selected source. Not used.

Address(hex): 0B

Register Name	*sts_priority_table*		Description	(RO) Bits [15:8] of the validated priority table.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				2nd highest priority validated source			

Bit No.	Description	Bit Value	Value Description
[7:4]	*Note used*	-	-
[3:0]	*2nd highest priority validated* Reports the input channel number of the 2nd highest priority validated source. Note that if an input is valid and it does not appear in this field, then the input may have been disallowed in register 30, 31h. Register 4B, bit 4 must be set to '1' for correct setting and reporting of the T4 DPLL priorities.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Less than 2 valid sources available. Input I1 is the 2nd highest priority valid source. Input I2 is the 2nd highest priority valid source. Input I3 is the 2nd highest priority valid source. Input I4 is the 2nd highest priority valid source. Input I5 is the 2nd highest priority valid source. Input I6 is the 2nd highest priority valid source. Input I7 is the 2nd highest priority valid source. Input I8 is the 2nd highest priority valid source. Input I9 is the 2nd highest priority valid source. Input I10 is the 2nd highest priority valid source. Input I11 is the 2nd highest priority valid source. Input I12 is the 2nd highest priority valid source. Input I13 is the 2nd highest priority valid source. Input I14 is the 2nd highest priority valid source. Not used.

Address(hex): 0C

Register Name	*sts_current_DPLL_frequency [7:0]*		Description	(RO) Bits [7:0] of the current DPLL frequency.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
current_DPLL_frequency[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*Bits [7:0] of current_DPLL_frequency* *When Bit 4 of register 4B = 0 the frequency of the Monitor DPLL is reported. When this Bit 4 = 1 the frequency of the T4 DPLL is reported.	-	See register description of *sts_current_DPLL_frequency* at address 0D hex.

Address(hex): 0D

Register Name	*sts_current_DPLL_frequency [15:8]*		Description	(RO) Bits [15:8] of the current DPLL frequency.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
current_DPLL_frequency[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*current_DPLL_frequency[15:8]* This value in this register is combined with the value in register 0C and register 07 to represent the current frequency offset of the DPLL. When bit 4 of register 4B = 0 the frequency of the Monitor DPLL path is reported. When this Bit 4 = 1 the frequency of the T4 DPLL is reported. The value is actually the DPLL integral path value so it can be viewed as an average frequency, where the rate of change is related to the DPLL bandwidth.	-	In order to calculate the ppm offset of the DPLL with respect to the crystal oscillator frequency, the value in register 07, 0D & 0C need to be concatenated. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec will give the value in ppm offset with respect to the XO frequency, allowing for any crystal calibration that has been performed, via registers 3C & 3D. If Bit 3 of register 3B is *High* then this value will freeze if the DPLL has been pulled to its min or max frequency.

Address(hex): 0E

Register Name	*sts_sources_valid*		Description	(RO) 8 least significant bits of the *sts_sources_valid* register.		Default Value	0000 0000
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* Bit indicating if I8 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I8 is invalid. Input I8 is valid.
6	*I7* Bit indicating if I7 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I7 is invalid. Input I7 is valid.
5	*I6* Bit indicating if I6 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I6 is invalid. Input I6 is valid.
4	*I5* Bit indicating if I5 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I5 is invalid. Input I5 is valid.
3	*I4* Bit indicating if I4 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I4 is invalid. Input I4 is valid.
2	*I3* Bit indicating if I3 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I3 is invalid. Input I3 is valid.
1	*I2* Bit indicating if I2 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I2 is invalid. Input I2 is valid.
0	*I1* Bit indicating if I1 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I1 is invalid. Input I1 is valid.

Address(hex): 0F

Register Name	*sts_sources_valid*		Description	(RO) 8 most significant bits of the *sts_sources_valid* register.		Default Value	0000 0000
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		I14	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-

Address(hex): 0F (continued)

Bit No.	Description	Bit Value	Value Description
5	*I14* Bit indicating if I14 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I14 is invalid. Input I14 is valid.
4	*I13* Bit indicating if I13 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I13 is invalid. Input I13 is valid.
3	*I12* Bit indicating if I12 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I12 is invalid. Input I12 is valid.
2	*I11* Bit indicating if I11 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I11 is invalid. Input I11 is valid.
1	*I10* Bit indicating if I10 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I10 is invalid. Input I10 is valid.
0	*I9* Bit indicating if I9 is valid. The input is valid if either it has no outstanding alarms, or it only has a soft frequency alarm.	0 1	Input I9 is invalid. Input I9 is valid.

Address(hex): 10 - 16

Register Name	*sts_reference_sources* *Input pairs (1 & 2)*		**Description**	(RO except for test when R/W) Reports any alarms active on inputs.		**Default Value**	0110 0110
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Address 10: Status of I2 Input *Address 11: Status of I4 Input* *Address 12: Status of I6 Input* *Address 13: Status of I8 Input* *Address 14: Status of I10 Input* *Address 15: Status of I12 Input* *Address 16: Status of I14 Input*				*Address 10: Status of I1 Input* *Address 11: Status of I3 Input* *Address 12: Status of I5 Input* *Address 13: Status of I7 Input* *Address 14: Status of I9 Input* *Address 15: Status of I11 Input* *Address 16: Status of I13 Input*			

Bit No.	Description	Bit Value	Value Description
7 & 3	*Out-of-band alarm (soft)* Soft out of band alarm bit for input. A "soft" alarm will not invalidate an input.	0 1	No alarm. Alarm armed. Alarm thresholds (range) set by register 49, or by register 4A, bits [7:4] if the input is currently selected.
6 & 2	*Out-of-band alarm (hard)* Hard out of band alarm bit for input. A "hard" alarm will invalidate an input.	0 1	No alarm. Alarm armed. Alarm thresholds set by register 49 bits [3:0], or by register 4A bits [3:0] if the input is currently selected.
5 & 1	*No activity alarm* Alarm indication from the activity monitors.	0 1	No alarm. Input has an active no activity alarm.

Address(hex): 10 – 16 (continued)

Bit No.	Description	Bit Value	Value Description
4 & 0	*Phase lock alarm* If the DPLL can not indicate that it is phase locked onto the current source within 100 seconds this alarm will be raised.	0 1	No alarm. Phase lock alarm.

Address(hex): 18 – 1E

Register Name	*cnfg_ref_selection_priority (1 & 2)*		Description	(R/W) Configures the relative priority of input sources I1 and I2.		Default Value	See Table 5 on page 9
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18: cnfg_ref_selection_priority_2 *Address 19: cnfg_ref_selection_priority_4* *Address 1A: cnfg_ref_selection_priority_6* *Address 1B: cnfg_ref_selection_priority_8* *Address 1C: cnfg_ref_selection_priority_10* *Address 1D: cnfg_ref_selection_priority_12* *Address 1E: cnfg_ref_selection_priority_14*				*Address 18: cnfg_ref_selection_priority_1* *Address 19: cnfg_ref_selection_priority_3* *Address 1A: cnfg_ref_selection_priority_5* *Address 1B: cnfg_ref_selection_priority_7* *Address 1C: cnfg_ref_selection_priority_9* *Address 1D: cnfg_ref_selection_priority_11* *Address 1E: cnfg_ref_selection_priority_13*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*cnfg_ref_selection_priority_2 - 14* This 4-bit value represents the relative priority of the input, for inputs I2 to I14. The smaller the number, the higher the priority; zero disables the input. Register 4B, bit 4 must be set to ‘1’ for correct setting and reporting of the T4 DPLL priorities.	0000 0001-1111	Input I2 - I14 unavailable for automatic selection. Input I2 to Input I14 (even no.s) priority value.
[3:0]	*cnfg_ref_selection_priority_1 - 13* This 4-bit value represents the relative priority of the input, for inputs I1 to I13 . The smaller the number, the higher the priority; zero disables the input. Register 4B, bit 4 must be set to ‘1’ for correct setting and reporting of the T4 DPLL priorities.	0000 0001-1111	Input I1 - I13 unavailable for automatic selection. Input I1 to Input I13 (odd no.s) priority value.

Address(hex): 20

Register Name	*cnfg_ref_source_frequency1*		Description	(R/W) Configuration of the frequency and input monitoring for input I1.		Default Value	0000 0000
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set to zero		*bucket_id_1*		Set to zero			

Bit No.	Description	Bit Value	Value Description
[7:6]	Set to zero	00	Set to zero
[5:4]	*bucket_id_1* Every input has its own Leaky Bucket type activity monitor. There are four possible configurations for each monitor- see register 50 to 5F. This 2-bit field selects the configuration used for input I1.	00 01 10 11	Input I1 uses activity monitor Configuration 0. Input I1 uses activity monitor Configuration 1. Input I1 uses activity monitor Configuration 2. Input I1 uses activity monitor Configuration 3.
[3:0]	Set to zero	0000	Set up for 8 kHz inputs only as AMI input.

Address(hex): 21

Register Name	*cnfg_ref_source_frequency2*		Description	(R/W) Configuration of the frequency and input monitoring for input I2		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set to zero		*bucket_id_2*		Set to zero			

Bit No.	Description	Bit Value	Value Description
[7:6]	Set to zero	00	Set to zero
[5:4]	*bucket_id_2* Every input has its own Leaky Bucket type activity monitor. There are four possible configurations for each monitor- see register 50 to 5F. This 2-bit field selects the configuration used for input I2.	00 01 10 11	Input I2 uses activity monitor Configuration 0. Input I2 uses activity monitor Configuration 1. Input I2 uses activity monitor Configuration 2. Input I2 uses activity monitor Configuration 3.
[3:0]	Set to zero	0000	Set up for 8 kHz inputs only as AMI input.

Address(hex): 22 – 2D

In the following table :

For register address 22 : <n> = 3
For register address 23 : <n> = 4
For register address 24 : <n> = 5
For register address 25 : <n> = 6
For register address 26 : <n> = 7
For register address 27 : <n> = 8
For register address 28 : <n> = 9
For register address 29 : <n> = 10
For register address 2A : <n> = 11
For register address 2B : <n> = 12
For register address 2C : <n> = 13
For register address 2D : <n> = 14

Register Name	*cnfg_ref_source_frequency_<n>*		Description	(R/W) Configuration of the frequency and input monitoring for input I<n>.		Default Value	See Table 5 on page 9
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
divn_<n>	*lock8k_<n>*	*bucket_id_<n>*		*reference_source_frequency_<n>*			

Bit No.	Description	Bit Value	Value Description
7	*divn_<n>* This bit selects whether or not input I<n> is divided in the programmable pre-divider prior to being input to the DPLL and frequency monitor- see register 46h & 47h (*cnfg_freq_divn*).	0 1	Input I<n> fed directly to DPLL and monitor. Input I<n> fed to DPLL and monitor via pre-divider.
6	*lock8k_<n>* This bit selects whether or not input I<n> is divided in the preset pre-divider prior to being input to the DPLL. This results in the DPLL locking to the reference after it has been divided to 8 kHz. This bit is ignored when *divn_<n>* is set (bit =1).	0 1	Input I<n> fed directly to DPLL. Input I<n> fed to DPLL via preset pre-divider.
[5:4]	*bucket_id_<n>* Every input has its own Leaky Bucket type activity monitor. There are four possible configurations for each monitor- see register 50 to 5F. This 2-bit field selects the configuration used for input I<n>.	00 01 10 11	Input I<n> uses activity monitor Configuration 0. Input I<n> uses activity monitor Configuration 1. Input I<n> uses activity monitor Configuration 2. Input I<n> uses activity monitor Configuration 3.

Address(hex): 22 (continued)

Bit No.	Description	Bit Value	Value Description
[3:0]	*reference_source_frequency_<n>* Programs the frequency of the reference source connected to input I<n>. If *divn_<n>* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011-1111	8 kHz. 1544/2048 kHz dependant on bit 2 in register 34 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used.

Address(hex): 30

Register Name	*cnfg_sts_remote_sources_valid*		Description	(R/W) Bits [7:0] of the remote sources valid register. A register used to disable sources that are invalid in another device in a redundancy pair.		Default Value	1111 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* - Bit enabling input I8 to be considered for locking to. If this bit is not set, then even if this input I8 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I8 disallowed. Locking to input I8 allowed.
6	*I7* - Bit enabling input I7 to be considered for locking to. If this bit is not set, then even if this input I7 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I7 disallowed. Locking to input I7 allowed.
5	*I6* - Bit enabling input I6 to be considered for locking to. If this bit is not set, then even if this input I6 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I6 disallowed. Locking to input I6 allowed.
4	*I5* - Bit enabling input I5 to be considered for locking to. If this bit is not set, then even if this input I5 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I5 disallowed. Locking to input I5 allowed.
3	*I4* - Bit enabling input I4 to be considered for locking to. If this bit is not set, then even if this input I4 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I4 disallowed. Locking to input I4 allowed.
2	*I3* - Bit enabling input I3 to be considered for locking to. If this bit is not set, then even if this input I3 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I3 disallowed. Locking to input I3 allowed.
1	*I2* - Bit enabling input I2 to be considered for locking to. If this bit is not set, then even if this input I2 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I2 disallowed. Locking to input I2 allowed.
0	*I1* - Bit enabling input I1 to be considered for locking to. If this bit is not set, then even if this input I1 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I1 disallowed. Locking to input I1 allowed.

Address(hex): 31

Register Name	*cnfg_sts_remote_sources_valid*		Description	(R/W) Bits [13:8] of the remote sources valid register. A register used to disable source that are invalid in another device in a redundancy pair.		Default Value	0011 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		I14	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
5	*I14* Bit enabling input I14 to be considered for locking to. If this bit is not set, then even if this input I14 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I14 disallowed. Locking to input I14 allowed.
4	*I13* Bit enabling input I13 to be considered for locking to. If this bit is not set, then even if this input I13 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I13 disallowed. Locking to input I13 allowed.
3	*I12* Bit enabling input I12 to be considered for locking to. If this bit is not set, then even if this input I12 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I12 disallowed. Locking to input I12 allowed.
2	*I11* Bit enabling input I11 to be considered for locking to. If this bit is not set, then even if this input I11 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I11 disallowed. Locking to input I11 allowed.
1	*I10* Bit enabling input I10 to be considered for locking to. If this bit is not set, then even if this input I10 is valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I10 disallowed. Locking to input I10 allowed.
0	*I9* Bit enabling input I9 to be considered for locking to. If this bit is not set, then even if this input I9 is valid, valid, it will still not appear in register 0A & 0B.	0 1	Locking to input I9 disallowed. Locking to input I9 allowed.

Address(hex): 33

Register Name	*Mon_DPLL_ref_source*		Description	(R/W) Register used for the selection of a particular reference source to the Monitor DPLL.		Default Value	0000 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				Mon_DPLL_ref_source			

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-

Address(hex): 33 (continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[3:0]	*Mon_DPLL_ref_source* Value representing the source to be selected for the Monitor DPLL. Ensure that register 34, bit 0 is set to "1".			0000/1111 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110	Should not be used. Select input I1. Select input I2. Select input I3. Select input I4. Select input I5. Select input I6. Select input I7. Select input I8. Select input I9. Select input I10. Select input I11. Select input I12. Select input I13. Select input I14.		

Address(hex): 34

Register Name	*cnfg_input_mode*		**Description**	(Bit 1 RO, otherwise R/W) Register controlling various input modes of the device.		**Default Value**	1100 0010*
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set to 0	*Set to 1*	*Set to 0*	*Set to 0*	*Set to 0*	*ip_sonsdhb*		*Set to 1*
Bit No.	**Description**			**Bit Value**	**Value Description**		
7,5,4,3	*Set to 0*			0	-		
6,0	*Set to 1*			1	-		
1	*Not used*			1	-		
2	*ip_sonsdhb* Bit to configure input frequencies to be either SONET or SDH derived. This applies only to selections of 0001 (bin) in the *cnfg_ref_source_ frequency* registers when the input frequency is either 1544 kHz or 2048 kHz. *The default value of this bit is taken from the value of the SONSDHB pin at power-up.			0 1	SDH- inputs set to 0001 expected to be 2048 kHz. SONET- inputs set to 0001 expected to be 1544 kHz		

Address(hex): 35

Register Name	*cnfg_T4_path*		Description	Register to configure the inputs and other features in the T4 path.		Default Value	0100 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set to 0	*T4_dig_feed-back*		*Set to 0*	*T4_forced_reference_source*			

Bit No.	Description	Bit Value	Value Description
7	*Set to 0*	0	-
6	*T4_dig_feedback* Bit to select digital feedback mode for the T4 DPLL.	0 1	T4 DPLL in analog feedback mode. T4 DPLL in digital feedback mode.
5	Not used.	-	-
4	*Set to 0*	0	

Address(hex): 36

Register Name	*cnfg_differential_inputs*		Description	(R/W) Configures the differential inputs to be PECL or LVDS type inputs.		Default Value	0000 0010
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						I6_PECL	*I5_LVDS*

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
1	*I6_PECL* Configures the I6 input to be compatible with either 3 V LVDS or 3 V PECL electrical levels.	0 1	I6 input LVDS compatible. I6 input PECL compatible (Default).
0	*I5_LVDS* Configures the I5 input to be compatible with either 3 V LVDS or 3 V PECL electrical levels.	0 1	I5 input LVDS compatible (Default). I5 input PECL compatible.

Address(hex): 37

Register Name	*cnfg_uPsel_pins*		Description	(RO) Register reflecting the value on the UPSEL device pins.	Default Value	0000 0010*	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					upsel_pins_value		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	*upsel_pins_value* This register always reflects the value present on the UPSEL pins of the device. At reset this is used to set the mode of the microprocessor interface. Following power-up, these pins have no further effect on the microprocessor interface, hence it is possible to use the pins and register combination as a general purpose input for software. *The default of this register is entirely dependent on the value of the pins at reset.	000 001 010 011 100 101 110 111	Not used. Interface in EPROM boot mode. Interface in Multiplexed mode. Interface in Intel mode. Interface in Motorola mode. Interface in Serial mode. Not used. Not used.

Address(hex): 3B

Register Name	*cnfg_int*		Description	(R/W) Register to freeze integral path in monitor DPLL	Default Value	1111 1011	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set to 0				Mon_lim_int			

Bit No.	Description	Bit Value	Value Description
7	*Set to 0*	0	-
[6:4]	Not used.	-	-
3	Mon_lim_int When set to 1 the integral path value of the monitor DPLL is limited or frozen when the monitor DPLL reaches either min or max frequency. This can be used to minimise subsequent overshoot when the DPLL is pulling in. Note that when this happens, the reported frequency value via *current_DPLL_freq* (registers 0C, 0D &07) is also frozen.	1 0	Monitor DPLL integral value frozen when pulled to max freq. range DPLL not frozen
[2:0]	Not used.	-	-

Address(hex): 3C

Register Name	*cnfg_nominal_frequency [7:0]*		Description	(R/W) Bits [7:0] of the register used to calibrate the crystal oscillator used to clock the device.		Default Value	1001 1001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
cnfg_nominal_frequency_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*cnfg_nominal_frequency_value[7:0]*	-	See register description of register 3D (*cnfg_nominal_frequency_value[15:8]*)

Address(hex): 3D

Register Name	*cnfg_nominal_frequency [15:8]*		Description	(R/W) Bits [15:8] of the register used to calibrate the crystal oscillator used to clock the device.		Default Value	1001 1001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
cnfg_nominal_frequency_value[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*cnfg_nominal_frequency_value[15:8]* This register is used in conjunction with register 3C to be able to offset the frequency of the crystal oscillator by up to +514 ppm and -771ppm. The default value represents 0 ppm offset from 12.800 MHz. This value is an unsigned integer.	-	In order to program the ppm offset of the crystal oscillator frequency, the value in 3C and 3D hex need to be concatenated. This value is a 2's complement signed integer. The value multiplied by 0.0196229 dec will give the value in ppm. To calculate the absolute value, the default (39321) needs to be subtracted.

Address(hex): 3E

Register Name	*cnfg_average_frequency [7:0]*		Description	(R/W) Bits [7:0] of the average frequency register.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
cnfg_average_frequency[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*average_frequency_value[7:0]*	-	See register 3F *cnfg_average_frequency* for details.

Address(hex): 3F

Register Name	Cnfg_average_frequency [15:8]		Description	(R/W) Bits [15:8] of the average frequency register.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
average_frequency_value[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*average_frequency[15:8]* This value in this register is combined with the value in register 3E and Bits [2:0] of register 40 to represent the average frequency of the Monitor DPLL. Also see register 40h bit 6. Register 40 , bit 5 must be set high.	-	In order to calculate average frequency of the monitor DPLL with respect to the crystal oscillator frequency, the value in this register and register 3Eh and Bits [2:0] of register 40h need to be concatenated. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec will give the value in ppm.

Address(hex): 40

Register Name	cnfg_averager_modes		Description	(R/W) Register to control the average modes of the monitor DPLL.		Default Value	1000 1000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
freq_averaging	*fast_averaging*	*Set to 1*	*Set to 0*	*Set to 1*	*average_frequency_value [18:16]*		

Bit No.	Description	Bit Value	Value Description
7	*freq_averaging* Bit to enable the frequency averager.	0 1	Additional averaging not done. Additional averaging carried out and reported.
6	*fast_averaging* Bit to control the rate of averaging of the frequency. Fast averaging gives a -3db response point of approximately 8 minutes. Slow averaging give a -3db response point of approximately 110 minutes.	0 1	Slow Holdover frequency averaging enabled. Fast Holdover frequency averaging enabled.
5	*Set to 1* *To allow the averaged frequency to be read out.*	1	-
4	*Set to 0*	0	-
3	*Set to 1*	1	-
[2:0]	*averager_frequency_value [18:16]*	-	See register 3F (*cnfg_average_frequency*) for details.

Address(hex): 41

Register Name	*cnfg_DPLL_freq_limit [7:0]*	Description	(R/W) Bits [7:0] of the DPLL frequency limit register.	Default Value	0111 0110		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DPLL_freq_limit_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*DPLL_freq_limit_value[7:0]* This register defines the extent of frequency offset to which either the Monitor or the T4 DPLL will track a source before limiting- i.e. it represents the pull-in range of the DPLLs. The offset of the device is determined by the frequency offset of the DPLL when compared to the offset of the external crystal oscillator clocking the device. If the oscillator is calibrated using register 3C & 3D, then this calibration is automatically taken into account. The DPLL frequency limit limits the offset of the DPLL when compared to the calibrated oscillator frequency.	-	In order to calculate the frequency limit in ppm, bits[1:0] of register 42h & bits[7:0] of register 41h need to be concatenated. This value is a unsigned integer and represents the limit, both positive and negative, in ppm. The value multiplied by 0.078 will give the value in ppm.

Address(hex): 42

Register Name	*cnfg_DPLL_freq_limit [9:8]*	Description	(R/W) Bits [9:8] of the DPLL frequency limit register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						DPLL_freq_limit_value[9:8]	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*DPLL_freq_limit_value[9:8]*	-	See register 41 (*cnfg_DPLL_freq_limit.*) for details.

Address(hex): 43

Register Name	*cnfg_interrupt_mask [7:0]*	Description	(R/W) Bits [7:0] of the interrupt mask register.	Default Value	0000 0000		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
I8	*I7*	*I6*	*I5*	*I4*	*I3*	*I2*	*I1*

Bit No.	Description	Bit Value	Value Description
7	*I8* Mask bit for input I8 interrupt.	0 1	Input I8 cannot generate interrupts. Input I8 can generate interrupts.
6	*I7* Mask bit for input I7 interrupt.	0 1	Input I7 cannot generate interrupts. Input I7 can generate interrupts.
5	*I6* Mask bit for input I6 interrupt.	0 1	Input I6 cannot generate interrupts. Input I6 can generate interrupts.

Address(hex): 43 (continued)

Bit No.	Description	Bit Value	Value Description
4	*I5* Mask bit for input I5 interrupt.	0 1	Input I5 cannot generate interrupts. Input I5 can generate interrupts.
3	*I4* Mask bit for input I4 interrupt.	0 1	Input I4 cannot generate interrupts. Input I4 can generate interrupts.
2	*I3* Mask bit for input I3 interrupt.	0 1	Input I3 cannot generate interrupts. Input I3 can generate interrupts.
1	*I2* Mask bit for input I2 interrupt.	0 1	Input I2 cannot generate interrupts. Input I2 can generate interrupts.
0	*I1* Mask bit for input I1 interrupt.	0 1	Input I1 cannot generate interrupts. Input I1 can generate interrupts.

Address(hex): 44

Register Name	*cnfg_interrupt_mask [15:8]*		Description	(R/W) Bits [15:8] of the interrupt mask register.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
MonDPLL_state	*Mon_ref_failed*	*I14*	*I13*	*I12*	*I11*	*I10*	*I9*

Bit No.	Description	Bit Value	Value Description
7	*MonDPLL_state* Mask bit for *MonDPLL_state* interrupt.	0 1	Operating state cannot generate interrupts. Operating state can generate interrupts.
6	*Mon_ref_failed* Mask bit for *Mon_ref_failed* interrupt.	0 1	Monitor DPLL reference failure cannot generate interrupts. Monitor DPLL reference failure can generate interrupts.
5	*I14* Mask bit for input I14 interrupt.	0 1	Input I14 cannot generate interrupts. Input I14 can generate interrupts.
4	*I13* Mask bit for input I13 interrupt.	0 1	Input I13 cannot generate interrupts. Input I13 can generate interrupts.
3	*I12* Mask bit for input I12 interrupt.	0 1	Input I12 cannot generate interrupts. Input I12 can generate interrupts.
2	*I11* Mask bit for input I11 interrupt.	0 1	Input I11 cannot generate interrupts. Input I11 can generate interrupts.
1	*I10* Mask bit for input I10 interrupt.	0 1	Input I10 cannot generate interrupts. Input I10 can generate interrupts.
0	*I9* Mask bit for input I9 interrupt.	0 1	Input I9 cannot generate interrupts. Input I9 can generate interrupts.

Address(hex): 45

Register Name	*cnfg_interrupt_mask [23:16]*		**Description**	(R/W) Bits [23:16] of the interrupt mask register.		**Default Value**	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set to 0	*T4_status*	*Set to 0*	*T4_inputs_ failed*	*AMI2_Viol*	*AMI2_LOS*	*AMI1_Viol*	*AMI1_LOS*

Bit No.	Description	Bit Value	Value Description
7	*Set to 0*	0	-
6	*T4_status* Mask bit for *T4_status* interrupt.	0 1	Change in T4 status cannot generate interrupts. Change in T4 status can generate interrupts.
5	*NSet to 0*	0	-
4	*T4_inputs_failed* Mask bit for *T4_inputs_failed* interrupt.	0 1	Failure of T4 inputs cannot generate interrupts. Failure of T4 inputs can generate interrupts.
3	*AMI2_Viol* Mask bit for *AMI2_Viol* interrupt.	0 1	Input I2 cannot generate AMI violation interrupts. Input I2 can generate AMI violation interrupts.
2	*AMI2_LOS* Mask bit for *AMI2_LOS* interrupt.	0 1	Input I2 cannot generate AMI LOS interrupts. Input I2 can generate AMI LOS interrupts.
1	*AMI1_Viol* Mask bit for *AMI1_Viol* interrupt.	0 1	Input I1 cannot generate AMI violation interrupts. Input I1 can generate AMI violation interrupts.
0	*AMI1_LOS* Mask bit for *AMI1_LOS* interrupt.	0 1	Input I1 cannot generate AMI LOS interrupts. Input I1 can generate AMI LOS interrupts.

Address(hex): 46

Register Name	*cnfg_freq_divn [7:0]*		**Description**	(R/W) Bits [7:0] of the division factor for inputs using the DivN feature.		**Default Value**	1111 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
divn_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*divn_value[7:0]*	-	See register 47 (*cnfg_freq_divn*) for details.

Address(hex): 47

Register Name	*cnfg_freq_divn [13:8]*		**Description**	(R/W) Bits [13:8] of the division factor for inputs using the DivN feature.		**Default Value**	0011 1111
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		divn_value[13:8]					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-

Address(hex): 47 (continued)

Bit No.	Description	Bit Value	Value Description
[5:0]	*divn_value[13:8]* This register, in conjunction with register 46 (*cnfg_ freq_divn*) represents the integer value by which to divide inputs that use the DivN pre-divider. The divn feature supports input frequencies up to a maximum of 100 MHz; therefore, the maximum value that should be written to this register is 30D3 hex (12499 dec). Use of higher DivN values may result in unreliable behaviour.	-	The input frequency will be divided by the value in this register plus 1. i.e. to divide by 8, program a value of 7.

Address(hex): 48

Register Name	*cnfg_monitors*		**Description**	(R/W) Configuration register controlling several input monitoring and switching options.		**Default Value**	0000 0101*
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set to 1	*los_flag_on_ TDO*	*Set to 0*	*Set to 0*	*Set to 0*	*Set to 0*	*freq_monitor_ soft_enable*	*freq_monitor_ hard_enable*

Bit No.	Description	Bit Value	Value Description
7	*Set to 1* To ensure the freq monitors are clocked directly from the crystal oscillator.	1	-
6	*los_flag_on_TDO* Bit to select whether the *mon_ref_fail* interrupt from the Monitor DPLL is flagged on the TDO pin. If enabled this will not strictly conform to the IEEE 1149.1 JTAG standard for the function of the TDO pin. When enabled the TDO pin will simply mimic the state of the *mon_ref_fail* interrupt status bit.	0 1	Normal mode, TDO complies with IEEE 1149.1. TDO pin used to indicate the state of the *main_ref_fail* interrupt status. This allows a system to have a hardware indication of a source failure very rapidly.
5,4,3,2	*Set to 0.*	0	-
1	freq_monitor_soft_enable Control to enable frequency monitoring of input reference sources using soft frequency alarms.	0 1	Soft frequency monitor alarms disabled. Soft frequency monitor alarms enabled.
0	*freq_monitor_hard_enable* Control to enable frequency monitoring of input reference sources using hard frequency alarms.	0 1	Hard frequency monitor alarms disabled. Hard frequency monitor alarms enabled.

Address(hex): 49

Register Name	*cnfg_freq_mon_threshold*		Description	(R/W) Register to set both the hard and soft frequency alarm limits for the monitors on the input reference sources.		Default Value	0010 0011
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
soft_frequency_alarm_threshold				*hard_frequency_alarm_threshold*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*soft_frequency_alarm_threshold* Threshold to trigger the soft frequency alarms in the *sts_reference_sources* registers. This is only used for monitoring.	-	To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of ±11.43 ppm.
[3:0]	*hard_frequency_alarm_threshold* Threshold to trigger the hard frequency alarms in the s *ts_reference_sources* registers, which can cause a reference source rejection.		To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0011 bin corresponds to an alarm limit of ±15.24 ppm.

Address(hex): 4A

Register Name	*cnfg_current_freq_mon_ threshold*		Description	(R/W) Register to set both the hard and soft frequency alarm limits for the monitors on the currently selected reference source.		Default Value	0010 0011
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
current_soft_frequency_alarm_threshold				*current_hard_frequency_alarm_threshold*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*current_soft_frequency_alarm_threshold* Threshold to trigger the soft frequency alarm in the *sts_reference_sources* register applying to the currently selected source.The currently selected source can be monitored for frequency using different limits to all other sources.	-	To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0010 bin corresponds to an alarm limit of ±11.43 ppm.
[3:0]	*current_hard_frequency_alarm_threshold* Threshold to trigger the hard frequency alarm in the *sts_reference_sources* register applying to the currently selected source.		To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by 3.81 ppm. The limit is symmetrical about zero. A value of 0011 bin corresponds to an alarm limit of ±15.24 ppm.

Address(hex): 4B

Register Name	*cnfg_registers_source_select*		Description	(R/W) Register to select the source of many of the registers.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
			T4orMon_select	*frequency_measurement_channel_select*			

Bit No.	Description	Bit Value	Value Description
[7:5]	Not used.	-	-
4	*T4orMon_select* Bit to select between the Monitor DPLL and T4 DPLL values for: registers 0A, 0B, 0C, 0D, 07, 18 to 1E, 77 and 78	0 1	Monitor DPLL registers selected. T4 DPLL registers selected.
[3:0]	*frequency_measurement_channel_select* Register to select which input channel the frequency measurement result in register 4C is taken from.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Not used- refers to no input channel. Frequency measurement taken from input I1. Frequency measurement taken from input I2. Frequency measurement taken from input I3. Frequency measurement taken from input I4. Frequency measurement taken from input I5. Frequency measurement taken from input I6. Frequency measurement taken from input I7. Frequency measurement taken from input I8. Frequency measurement taken from input I9. Frequency measurement taken from input I10. Frequency measurement taken from input I11. Frequency measurement taken from input I12. Frequency measurement taken from input I13. Frequency measurement taken from input I14. Not used- refers to no input channel.

Address(hex): 4C

Register Name	*sts_freq_measurement*		Description	(R/W) Register from which the frequency measurement result can be read.		Default Value	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
freq_measurement_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*freq_measurement_value* This represents the value of the frequency measurement on the channel number selected in register 4B. This value will represent the offset in frequency from the external crystal oscillator . Ensure register 48, bit 7 = 1	-	This is an 8-bit 2's complement signed integer. To calculate the offset in ppm of the selected input channel, this value should be multiplied by 3.81 ppm.

Address(hex): 4D

Register Name	*cnfg_DPLL_soft_limit*		Description	(R/W) Register to program the soft frequency limit of the two DPLLs. Exceeding this limit will have no effect beyond triggering a flag.		Default Value	1000 1110
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
freq_lim_ ph_loss	*DPLL_soft_limit_value*						

Bit No.	Description	Bit Value	Value Description
7	*freq_lim_ph_loss* Bit to enable the phase lost indication when the DPLL hits its hard frequency limit as programmed in register 41h & 42h *(cnfg_DPLL_freq_limit*). This results in the DPLL entering the phase lost state any time the DPLL tracks to the extent of its hard limit. It applies to both the Monitor DPLL and the T4 DPLL	0 1	Phase lost/locked determined normally. Phase lost force when DPLL tracks to hard limit.
[6:0]	*DPLL_soft_limit_value* Register to program to what extent either of the DPLLs tracks a source before raising its soft frequency alarm flag (Bits 5 and 4 of register 09h). This offset is compared to the crystal oscillator frequency taking into account any programmed calibration from registers 3C & 3D.	-	To calculate the ppm offset multiply this 7-bit value by 0.628 ppm. The limit is symmetrical about zero. A value of 0001110 bin is equivalent to ±8.79 ppm.

Address(hex): 50

Register Name	*cnfg_upper_threshold_0*		Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 0.		Default Value	0000 0110
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
upper_threshold_0_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_0_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 53h, in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_0_value,* the activity monitor raises an input inactivity alarm.	00000001 to 11111111	Value at which the Leaky Bucket will raise an inactivity alarm.

Address(hex): 51

Register Name	*cnfg_lower_threshold_0*		Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 0.		Default Value	0000 0100
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
lower_threshold_0_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_0_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 53h, in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_0_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	00000000 to 11111111	Value at which the Leaky Bucket will reset an inactivity alarm.

Address(hex): 52

Register Name	*cnfg_bucket_size_0*		Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 0.		Default Value	0000 1000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
bucket_size_0_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_0_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 53h, in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	00000001 to 11111111	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address(hex): 53

Register Name	*cnfg_decay_rate_0*		**Description**	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 0.		**Default Value**	0000 0001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						decay_rate_0_value	

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:2]	Not used.	-	-
[1:0]	*decay_rate_0_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address(hex): 54

Register Name	*cnfg_upper_threshold_1*		**Description**	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 1.		**Default Value**	0000 0110
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
upper_threshold_1_value							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*upper_threshold_1_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 57h, in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_1_value,* the Leaky Bucket raises an input inactivity alarm.	00000001 to 11111111	Value at which the Leaky Bucket will raise an inactivity alarm.

Address(hex): 55

Register Name	*cnfg_lower_threshold_1*		Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 1.		Default Value	0000 0100
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_1_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_1_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 57h, in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_1_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	00000000 to 11111111	Value at which the Leaky Bucket will reset an inactivity alarm.

Address(hex): 56

Register Name	*cnfg_bucket_size_1*		Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 1.		Default Value	0000 1000
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_1_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_1_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 57h, in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	00000001 to 11111111	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address(hex): 57

Register Name	*cnfg_decay_rate_1*		Description	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 1.		Default Value	0000 0001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						decay_rate_1_value	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_1_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address(hex): 58

Register Name	*cnfg_upper_threshold_2*		Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 2.		Default Value	0000 0110
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
upper_threshold_2_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_2_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 5Bh, in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_2_value,* the Leaky Bucket raises an input inactivity alarm.	00000001 to 11111111	Value at which the Leaky Bucket will raise an inactivity alarm.

Address(hex): 59

Register Name	*cnfg_lower_threshold_2*		**Description**	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 2.		**Default Value**	0000 0100
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
lower_threshold_2_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_2_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 5Bh, in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_2_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	00000000 to 11111111	Value at which the Leaky Bucket will reset an inactivity alarm.

Address(hex): 5A

Register Name	*cnfg_bucket_size_2*		**Description**	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 2.		**Default Value**	0000 1000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
bucket_size_2_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_2_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 5Bh, in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	00000001 to 11111111	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address(hex): 5B

Register Name	*cnfg_decay_rate_2*		Description	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 2.		Default Value	0000 0001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						decay_rate_2_value	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_2_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 5Fh, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address(hex): 5C

Register Name	*cnfg_upper_threshold_3*		Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 3.		Default Value	0000 0110
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
upper_threshold_3_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_3_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 5Fh, in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_3_value,* the Leaky Bucket raises an input inactivity alarm.	00000001 to 11111111	Value at which the Leaky Bucket will raise an inactivity alarm.

Address(hex): 5D

Register Name	*cnfg_lower_threshold_3*		**Description**	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 3.		**Default Value**	0000 0100
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
lower_threshold_3_value							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*lower_threshold_3_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 5Fh, in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_3_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	00000000 to 11111111	Value at which the Leaky Bucket will reset an inactivity alarm.

Address(hex): 5E

Register Name	*cnfg_bucket_size_3*		**Description**	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 3.		**Default Value**	0000 1000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
bucket_size_3_value							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*bucket_size_3_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in register 5Fh, in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	00000001 to 11111111	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address(hex): 5F

Register Name	*cnfg_decay_rate_3*		Description	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 3.		Default Value	0000 0001
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_3_value	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_3_value* The Leaky Bucket type activity monitor operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address(hex): 60 – 62

Set all bits to zero to minimise power consumption

Address(hex): 63

Register Name	*cnfg_output_enab (TO1 & TO2)*		Description	(R/W) Register to enable the frequencies available on outputs.		Default Value	1111 0110
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set to 0	*Set to 0*	*TO1_en*	*TO2_en*	*Set to 0*	*Set to 0*	*Set to 0*	*Set to 0*

Bit No.	Description	Bit Value	Value Description
7,6,3,2,1,0	*Set to 0* to minimise power	0	-
5	*TO1_en* Register bit to enable the BITS output from the TO1.	0 1	Output TO1 disabled. Output TO1 enabled.
4	*TO2_en* Register bit to enable the AMI composite clock output from TO2.	0 1	Output TO2 disabled. Output TO2 enabled.

Address(hex): 64

Register Name	*cnfg_T4_DPLL_frequency*		Description	(R/W) Register to configure the T4 DPLL and several other parameters for the T4 path.		Default Value	0000 0001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Auto_squelch_T4	*AMI_op_duty*	*T4_op_SONSDH*		*T4_DPLL_Enable*		

Bit No.	Description	Bit Value	Value Description
7, 3	Not used.	-	-
6	*Auto_squelch_T4* Register bit to automatically squelch the T4 outputs on TO1 and TO2 when the T4 inputs have failed.	0 1	Outputs TO1 and TO2 enabled as in register 63h Outputs TO1 and TO2 disabled when T4 inputs fail.
5	*AMI_op_duty* Register bit to configure whether the composite clock output of TO2 is 50:50 or 5:8 duty cycle.	0 1	TO2 output 50:50 duty cycle. TO2 output 5:8 duty cycle.
4	*T4_op_SONSDH* Register bit to configure the BITS output on TO1 to be either SONET or SDH frequency. Check that register 35h, bit 4 is set to 0, otherwise this bit is ignored and SONET/SDH selection for TO1 is controlled by register 34h, bit 2. Default set by SONSDHB pin - same as register 34 bit 2.	0 1	TO1 output 2.048 MHz (SDH). TO1 output 1.544 MHz (SONET).
[2:0]	*T4_DPLL_frequency* Register to control the system clock driving the T4 DPLL	000 001 010- 111	T4 DPLL squelched (clock off). T4 DPLL enabled (clock on). Do Not Use

Address(hex): 65

Register Name	*cnfg_T4_meas_phase*		Description	(R/W) Register to configure the T4 phase detector to measure the phase between 2 inputs		Default Value	0000 0001
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
T4_meas_phas	*Set to 0*				*Set to 0*	*Set to 0*	*Set to 1*

Bit No.	Description	Bit Value	Value Description
7	*T4_meas_phas* Register bit to control the feature to use the T4 path to measure phase difference between the Monitor DPLL input and the selected T4 input.	0 1	Normal- T4 Path normal operation. T4 DPLL disabled, T4 phase detector used to measure phase between selected Monitor DPLL input and the selected T4 input.
6, 2, 1	*Set to 0*	0	-
5,4,3	Not used.	0	-
0	*Set to 1*	1	-

Address(hex): 66

Register Name	*cnfg_T4_DPLL_bw*		**Description**	(R/W) Register to configure the bandwidth of the T4 DPLL.		**Default Value**	0000 0000
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
						T4_DPLL_bandwidth	

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:2]	Not used.	-	-
[1:0]	*T4_DPLL_bandwidth* Register to configure the bandwidth of the T4 DPLL.	00 01 10 11	T4 DPLL 18 Hz bandwidth. T4 DPLL 35 Hz bandwidth. T4 DPLL 70 Hz bandwidth. Not used.

Address(hex): 67

Register Name	*cnfg_Mon_DPLL_bw*		**Description**	(R/W) Register to configure the bandwidth of the Monitor DPLL		**Default Value**	0000 1011
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
			Monitor_DPLL_bandwidth				

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:5]	Not used.	0	-
[4:0]	*Monitor_DPLL_bandwidth* Register to configure the bandwidth of the Monitor DPLL	00000 00001 00010 00011 00100 00101 00110 01111 01000 01001 01010 01011 01100 01101 01110 01111 10000 10001 All other values	Mon DPLL 0.5 mHz locked bandwidth. Mon DPLL 1 mHz locked bandwidth. Mon DPLL 2 mHz locked bandwidth. Mon DPLL 4 mHz locked bandwidth. Mon DPLL 8 mHz locked bandwidth. Mon DPLL 15 mHz locked bandwidth. Mon DPLL 30 mHz locked bandwidth. Mon DPLL 60 mHz locked bandwidth. Mon DPLL 0.1 Hz locked bandwidth. Mon DPLL 0.3 Hz locked bandwidth. Mon DPLL 0.6 Hz locked bandwidth. Mon DPLL 1.2 Hz locked bandwidth. Mon DPLL 2.5 Hz locked bandwidth. Mon DPLL 4 Hz locked bandwidth. Mon DPLL 8 Hz locked bandwidth. Mon DPLL 18 Hz locked bandwidth. Mon DPLL 35 Hz locked bandwidth. Mon DPLL 70 Hz locked bandwidth. Not used.

Address(hex): 6A

Register Name	*Cnfg_T4_DPLL_damping*		Description	(R/W) Register to configure the damping factor of the T4 DPLL		Default Value	0001 0011
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Set to 0	*Set to 0*	*Set to 1*		*T4_damping*		
Bit No.	**Description**			**Bit Value**	**Value Description**		
7,3	Not used.			-	-		
[6:4]	*Set to 001*			001	-		
[2:0]	*T4_damping* Register to configure the damping factor of the T4 DPLL. The bit values corresponds to different damping factors, depending on the bandwidth selected. Damping factor of 5 being the default (011). The gain peak for the damping factors given in the value description (right) are tabulated below.			001 010 011 100 101 000 110 111	T4 DPLL damping factor at the following bandwidths frequency selections: *18 Hz* / *35 Hz* / *70 Hz* 1.2 / 1.2 / 1 2.5 / 2.5 / 2.5 5 / 5 / 5 5 / 10 / 10 5 / 10 / 20 Not used. Not used. Not used.		

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Address(hex): 6B

Register Name	*Cnfg_Mon_DPLL_damping*		Description	(R/W) Register to configure the damping factor of the Monitor DPLL, along with the gain of the Phase Detector 2 in some modes.		Default Value	0001 0011
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Set to 0	*Set to 0*	*Set to 1*		*Mon DPLL damping*		
Bit No.	**Description**			**Bit Value**	**Value Description**		
7,3	Not used.			-	-		
[6:4]	*Set to 001*			001	-		
[2:0]	*Mon_DPLL_damping* Register to configure the damping factor of the Monitor DPLL. The bit values corresponds to different damping factors, depending on the bandwidth selected. Damping factor of 5 being the default (011). The gain peak for the Damping Factors given in the Value Description (right) are as tabulated above in the register 6A description. .			001 010 011 100 101 000/110/111	Monitor DPLL damping factor at the following bandwidths frequency selections: *<4 Hz* / *8 Hz* / *18 Hz* / *35 Hz* / *70 Hz* 5 / 2.5 / 1.2 / 1.2 / 1.2 5 / 5 / 2.5 / 2.5 / 2.5 5 / 5 / 5 / 5 / 5 5 / 5 / 5 / 10 / 10 5 / 5 / 5 / 10 / 20 Not used.		

Address(hex): 73

Register Name	*cnfg_phase_loss_limit*		Description	(R/W) Register to configure some of the parameters of the Monitor DPLL phase detector.		Default Value	1010 0010
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
fine_limit_en	*noact_ph_loss*	*narrow_en*			*phase_loss_fine_limit*		

Bit No.	Description	Bit Value	Value Description
7	*fine_limit_en* Register bit to enable the *phase_loss_fine_limit* Bits [2:0]. When disabled, phase lock/loss is determined by the other means within the device. This must be disabled when multi-UI jitter tolerance is required, see register 74h, *cnfg_phase_loss_course_limit* .	0 1	Phase loss indication only triggered by other means. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_fine_limit* , Bits [2:0].
6	*noact_ph_loss* The DPLL detects that an input has failed very rapidly. Normally, when the DPLL detects this condition, it does not consider phase lock to be lost and will phase lock to the nearest edge (±180°) when a source becomes available again, hence giving tolerance to missing cycles. If phase loss is indicated, then frequency and phase locking is instigated (±360° locking). This bit can be used to force the DPLL to indicate phase loss immediately when no activity is detected.	0 1	No activity on reference does not trigger phase lost indication. No activity triggers phase lost indication. It is recommended that it should be set = 1 when use is made of the *T4_DPLL_Lock* lock indication bit (register 09h, bit 6).
5	*narrow_en* (test control bit) Set to 1 (default value)	0 1	 Set to 1
[4:3]	Not used.	-	-
[2:0]	*phase_loss_fine_limit* When enabled by Bit 7, this register coarsely sets the phase limit at which the device indicates phase lost or locked. The default value of 2 (010) gives a window size of around ±(90° to 180°). The phase position of the inputs to the DPLL has to be within the window limit for 1 to 2 seconds before the device indicates phase lock. If it is outside the window for any time then phase loss is immediately indicated. For most cases the default value of 2 (010) is satisfactory. The window size changes in proportion to the value, so a value of 1 (001) will give a narrow phase acceptance or lock window of approximately ±(45° to 90°).	000 001 010 011 100 101 110 111	Do not use. Indicates phase loss continuously. Small phase window for phase lock indication. Recommended value.))) Larger phase window for phase lock indication.))

Address(hex): 74

Register Name	*cnfg_phase_loss_coarse_limit*		**Description**	(R/W) Register to configure some of the parameters of the Monitor DPLL phase detector.		**Default Value**	1000 0101
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
coarse_lim-phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
7	*coarse_lim_phaseloss_en* Register bit to enable the coarse phase detector, whose range is determined by *phase_loss_coarse_limit* Bits [3:0]. This register sets the limit in the number of input clock cycles (UI) that the input phase can move by before the DPLL indicates phase lost.	0 1	Phase loss not triggered by the coarse phase lock detector. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_coarse_limit* , Bits [3:0].
6	*wide_range_en* To enable the device to be tolerant to large amounts of applied jitter and still do direct phase locking at the input frequency rate (up to 77.76 MHz), a wide range phase detector and phase lock detector is employed. This bit enables the wide range phase detector. This allows the device to be tolerant to, and therefore keep track of, drifts in input phase of many cycles (UI). The range of the phase detector is set by the same register used for the phase loss coarse limit (Bits [3:0]).	0 1	Wide range phase detector off. Wide range phase detector on.
5	*multi_ph_resp* Enables the phase result from the coarse phase detector to be used in the DPLL algorithm. Bit 6 should also be set when this is activated. The coarse phase detector can measure and keep track over many thousands of input cycles, thus allowing excellent jitter and wander tolerance. This bit enables that phase result to be used in the DPLL algorithm, so that a large phase measurement gives a faster pull-in of the DPLL. If this bit is not set then the phase measurement is limited to ±360° which can give a slower pull-in rate at higher input frequencies, but could also be used to give less overshoot. Setting this bit in direct locking mode, for example with a 19.44 MHz input, could be used to give the same dynamic response as a 19.44 MHz input used with 8 k locking mode, where the input is divided down internally to 8 kHz first.	0 1	DPLL phase detector limited to ±360° (±1 UI). However it will still remember its original phase position over many thousands of UI if Bit 6 is set. DPLL phase detector also uses the full coarse phase detector result. It can now measure up to: ±360° X 8191 UI = ±2,948,760°.
4	Not used.	-	-
[3:0]	*phase_loss_coarse_limit* Sets the range of the coarse phase loss detector and the coarse phase detector. When locking to a high frequency signal and jitter tolerance greater than ± 0.5 UI is required, then the DPLL can be configured to track phase errors over many input clock periods. This is particularly useful with very low bandwidths. This register configures how many UI over which the input phase can be tracked. It also sets the range of the coarse phase loss detector, which can be used with or without the multi-UI phase capture range capability. This register value is used by Bits 6 and 7.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100-1111	Input phase error tracked over ±1 UI. Input phase error tracked over ±3 UI. Input phase error tracked over ±7 UI. Input phase error tracked over ±15 UI. Input phase error tracked over ±31 UI. Input phase error tracked over ±63 UI. Input phase error tracked over ±127 UI. Input phase error tracked over ±255 UI. Input phase error tracked over ±511 UI. Input phase error tracked over ±1023 UI. Input phase error tracked over ±2047 UI. Input phase error tracked over ±4095 UI. Input phase error tracked over ±8191 UI.

Address(hex): 76

Register Name	*cnfg_phasemon*		Description	(R/W) Register to configure the noise rejection function for low frequency inputs.	Default Value	0000 0110	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ip_noise_ window		*Set to 0*					

Bit No.	Description	Bit Value	Value Description
7	*ip_noise_window* Register bit to enable a window of 5% tolerance around low-frequency inputs (2, 4 and 8 kHz). This feature ensures that any edge caused by noise outside the 5% window where the edge is expected will not be considered within the DPLL. This reduces any possible phase hit when a low-frequency connection is removed and contact bounce is possible.	0 1	DPLL considers all edges for phase locking. DPLL ignores input edges outside a 95% to 105% window.
6,4,3,2,1,0	Not used.	-	-

Address(hex): 77

Register Name	*sts_current_phase [7:0]*		Description	(RO) Bits [7:0] of the current phase register.	Default Value	0000 0000	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
current_phase[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*current_phase* Bits [7:0] of the current phase register. See register 78h *sts_current_phase [15:8]* for details.	-	See register 78h *sts_current_phase [15:8]* for details.

Address(hex): 78

Register Name	*sts_current_phase [15:8]*		Description	(RO) Bits [15:8] of the current phase register.	Default Value	0000 0000	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
current_phase[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*current_phase* Bits [15:8] of the current phase register. This register is used to read either from the phase detector of either the Monitor DPLL or the T4 DPLL, according to register 4Bh bit 4 *T4orMon_select*. The value is averaged in the phase averager before being made available. The averager -3dB pole is normally at 100Hz, but is 200Hz for 70Hz bandwidths.	-	The value in this register should be concatenated with the value in register 77h *sts_current_phase [7:0]* . This 16-bit value is a 2's complement signed integer. The value multiplied by 0.707 is the averaged value of the current phase error, in degrees, as measured at the DPLL's phase detector.

Address(hex): 7D

Register Name	*cnfg_interrupt*		Description	(R/W) Register to configure interrupt output.		Default Value	0000 0010
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					GPO_en	*tristate_en*	*int_polarity*

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
2	*GPO_en* (Interrupt General Purpose Output). If the interrupt output pin is not required, then setting this bit will allow the pin to be used as a general purpose output. The pin will be driven to the state of the polarity control bit, *int_polarity* .	0 1	Interrupt output pin used for interrupts. Interrupt output pin used for GPO purpose.
1	*tristate_en* The interrupt can be configured to be either connected directly to a processor, or wired together with other sources.	0 1	Interrupt pin always driven when inactive. Interrupt pin only driven when active, High-impedance when inactive.
0	*int_polarity* The interrupt pin can be configured to be active *High* or *Low* .	0 1	Active *Low* - pin driven *Low* to indicate active interrupt. Active *High* - pin driven *High* to indicate active interrupt.

Address(hex): 7E

Register Name	*cnfg_protection*		Description	(R/W) Protection register to protect against erroneous software writes.		Default Value	1000 0101
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
protection_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*protection_value* This register can be used to ensure that the software writes a specific value to this register, before being able to modify any other register in the device. Three modes of protection are offered, (i) protected (ii) fully unprotected (iii) single unprotected. When protected, no other register in the device can be written to. When fully unprotected, any writeable register in the device can be written to. When single unprotected, only one register can be written before the device automatically re-protects itself.	0000 0000 - 1000 0100 1000 0101 1000 0110 1000 0111 - 1111 1111	Protected mode. Fully unprotected. Single unprotected. Protected mode.

Address(hex): 7F

Register Name	*cnfg_uPsel*		Description	(R/W)* Register reflecting the value on the UPSEL device pins following reset, and writeable in EPROM mode.		Default Value	0000 0000**
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					upsel_value		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	*upsel_value* This register defaults to reflecting the value present on the UPSEL pins of the device at reset. At reset this is used to set the mode of the microprocessor interface. Following power-up, these pins have no further effect on the microprocessor interface. *In order that the device can be "booted" from an EPROM and subsequently communicate with a processor, this register is programmable in EPROM mode. The value programmed in location 7F of the EPROM will be the value loaded into this register. **The default of this register is entirely dependent on the value of the pins at reset.	000 001 010 011 100 101 110 111 (value at reset)	Not used. Interface in EPROM boot mode. Interface in Multiplexed mode. Interface in Intel mode. Interface in Motorola mode. Interface in Serial mode. Not used. Not used.

All not mentioned addresses should not be written to.

Electrical Specifications

JTAG

The JTAG connections on the ACS8514 allow a full boundary scan to be made. The JTAG implementation is fully compliant to IEEE 1149.1[5], with the following minor exceptions, and the user should refer to the standard for further information.

1. The output boundary scan cells do not capture data from the core, and so do not support INTEST. However this does not affect board testing.
2. In common with some other manufacturers, pin TRST is internally pulled *Low* to disable JTAG by default. The standard is to pull *High* . The polarity of TRST is as the standard: TRST *High* to enable JTAG boundary scan mode, TRST *Low* for normal operation.

The JTAG timing diagram is shown in Figure 14 .

Over-voltage Protection

The ACS8514 may require Over-Voltage Protection on input reference clock ports according to ITU recommendation K.41[16]. Semtech protection devices are recommended for this purpose (see separate Semtech data book).

ESD Protection

Suitable precautions should be taken to protect against electrostatic damage during handling and assembly. This device incorporates ESD protection structures that protect the device against ESD damage at ESD input levels up to at least +/2kV using the Human Body Model (HBD) MIL-STD-883D Method 3015.7, for all pins except pins 24 & 25 (AMI inputs) which are protected up to at least +/- 1kV.

Latchup Protection

This device is protected against latchup for input currents pulses of magnitude up to at least +/- 100mA according to JEDEC Standard No.78 August 1997.

Figure 14 JTAG Timing

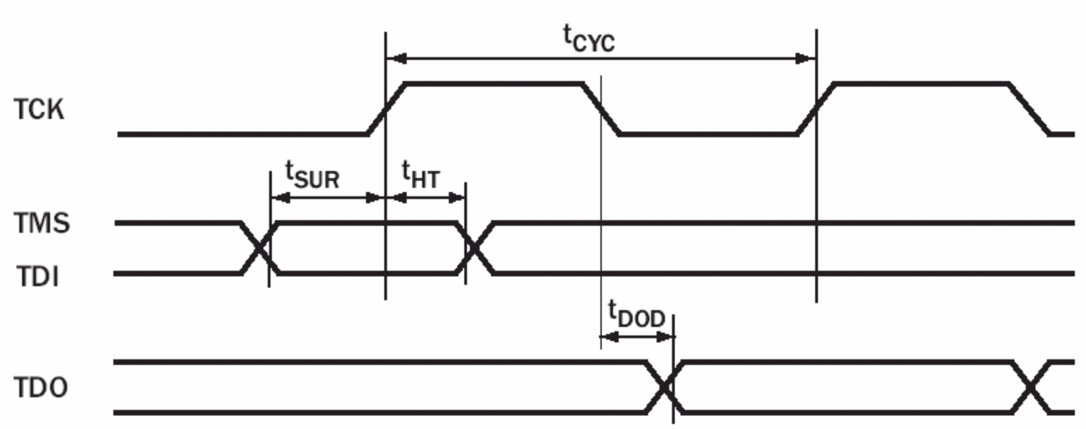


Table 20 JTAG Timing (for use with Figure 14)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Cycle Time	t_{CYC}	50	-	-	ns
TMS/TDI to TCK rising edge time	t_{SUR}	3	-	-	ns
TCK rising to TMS/TDI hold time	t_{HT}	23	-	-	ns
TCK falling to TDO valid	t_{DOD}	-	-	5	ns

Maximum Ratings

Important Note: The Absolute Maximum Ratings, Table 21, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 21 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage VDDa, VDDb, VDDc, VDDd, VD1+, VD2+, VD3+, VA1+, VA2+, VA3+, VAMI+, VDD_DIFFa, VDD_DIFFb	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	Vin	-	5.5	V
Output Voltage (non-supply pins)	Vout	-	5.5	V
Ambient Operating Temperature Range	TA	-40	+85	°C
Storage Temperature	Tstor	-50	+150	°C

Operating Conditions

Table 22 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply (dc voltage) VDDa, VDDb, VDDc, VDDd, VD1+, VD2+, VD3+, VA1+, VA2+, VA3+, VAMI+, VDD_DIFFa, VDD_DIFFb	VDD	3.0	3.3	3.6	V
Power Supply (dc voltage) VDD5	VDD5	3.0	3.3/5.0	5.5	V
Ambient Temperature Range	TA	-40	-	+85	°C
Supply Current (Typical - one 19 MHz output)	IDD	-	130	222	mA
Total Power Dissipation	PTOT	-	430	800	mW

DC Characteristics

Across all operating conditions, unless otherwise stated

Table 23 DC Characteristics: TTL Input Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Input Current	I_{IN}	-	-	10	µA

Table 24 DC Characteristics: TTL Input Port with Internal Pull-up

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-up Resistor	PU	30	-	80	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 25 DC Characteristics: TTL Input Port with Internal Pull-down

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-down Resistor	PU	30	-	80	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 26 DC Characteristics: TTL Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
Vout *Low* (Iol = 4mA)	Vol	0	-	0.4	V
Vout *High* (Ioh = 4mA)	Voh	2.4	-	-	V
Drive Current	ID	-	-	4	mA

Table 27 DC Characteristics: PECL Input Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Input *Low* Voltage Differential Inputs (Note (ii))	VILPECL	VDD-2.5	-	VDD-0.5	V
PECL Input *High* Voltage Differential Inputs (Note (ii))	VIHPECL	VDD-2.4	-	VDD-0.4	V
Input Differential Voltage	VIDPECL	0.1	-	1.4	V
PECL Input *Low* Voltage Single-ended Input (Note (iii))	VILPECL_S	VDD-2.4	-	VDD-1.5	V
PECL Input *High* Voltage Single-ended Input (Note (iii))	VILPECL_S	VDD-1.3	-	VDD-0.5	V
Input *High* Current Input Differential Voltage VID = 1.4V	IIHPECL	-10	-	+10	µA
Input *Low* Current Input Differential Voltage VID = 1.4V	IILPECL	-10	-	+10	µA

Notes:

(i) Unused differential input ports should be left floating and set in LVDS mode, or the positive and negative inputs tied to VDD and GND respectively.

(ii) Assuming a differential input voltage of at least 100 mV.

(iii) Unused differential input terminated to VDD -1.4 V.

Figure 15 Recommended Line Termination for PECL Input Ports

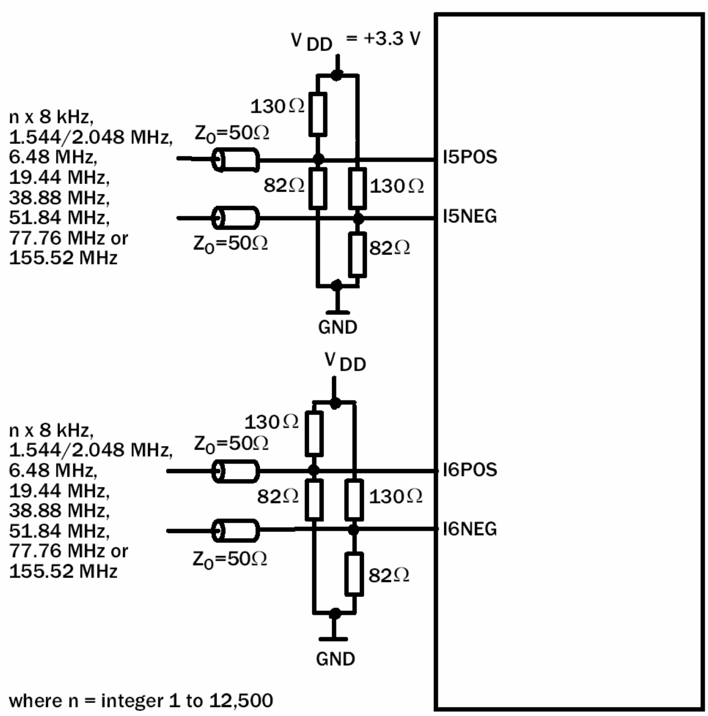
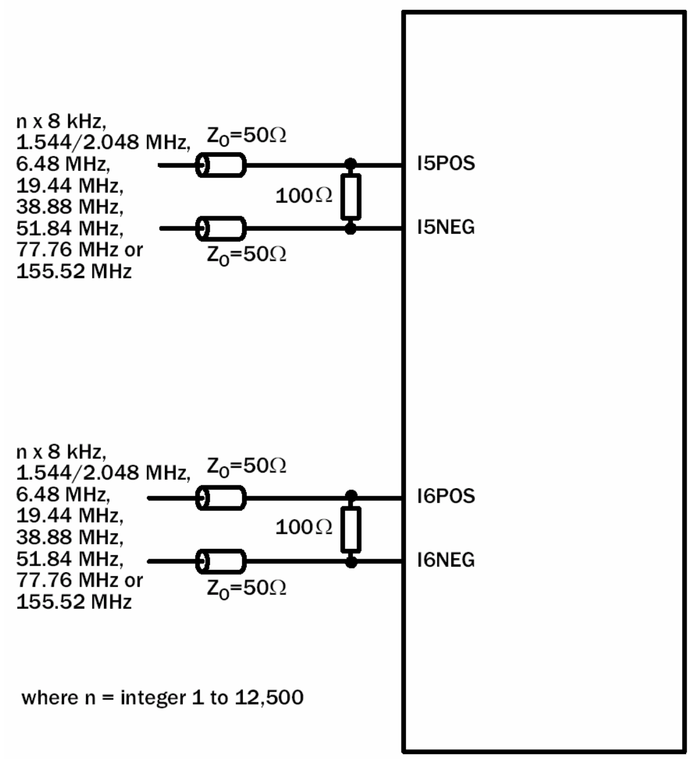


Table 28 DC Characteristics: LVDS Input Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS Input Voltage Range Differential Input Voltage = 100 mV	VVRLVDS	0	-	2.40	V
LVDS Differential Input Threshold	VDITH	-100	-	+100	mV
LVDS Input Differential Voltage	VIDLVTSDS	0.1	-	1.4	V
LVDS Input Termination Resistance Must be placed externally across the LVDS ± input pins of ACS8514. Resistor should be 100Ω with 5% tolerance	RTERM	95	100	105	Ω

Figure 16 Recommended Line Termination for LVDS Input Ports



DC Characteristics: AMI Input/Output Port

(Across all operating Conditions, unless otherwise stated.)

The Alternate Mark Inversion (AMI) signal is DC balanced and consists of positive and negative pulses with a peak-to-peak voltage of 2.0 ±0.2 V.

The electrical specifications are taken from option a) of Table 2/G.703 - Digital 64 kbit/s centralized clock interface, from ITU G.703[6].

The electrical characteristics of the 64 kbits/s interface are as follows:

Nominal bit rate: 64 kbits/s. The tolerance is determined by the network clock stability.

There should be a symmetrical pair carrying the composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

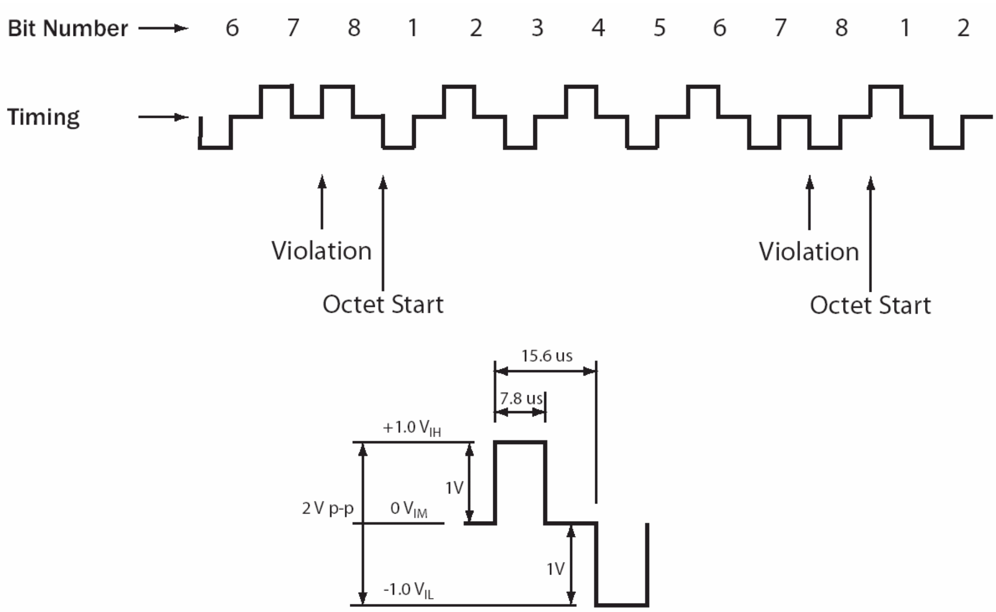
Over-voltage protection requirement: refer to Recommendation K.41[15]

Code conversion rules:
The data signals are coded in AMI code with 100% duty cycle. The composite clock timing signals convey the 64 kHz bit-timing information using AMI coding with a 50% to 70% duty ratio and the 8 kHz octet phase information by introducing violations in the code rule. The structure of the signals and voltage level are shown in Figure 17 , Figure 18 and Figure 19 .

Table 29 DC Characteristics: AMI Input/Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Pulse Width	t_{PW}	1.56	7.8	14.04	*m*s
Input Pulse Rise/Fall Time	$t_{R/F}$	-	-	5	*m*s
AMI Input Voltage *High*	$V_{IH\ AMI}$	2.5	-	VDD + 0.3	V
AMI Input Voltage *Middle*	$V_{IM\ AMI}$	1.5	1.65	1.8	V
AMI Input Voltage *Low*	$V_{IL\ AMI}$	0	-	1.4	V
AMI Output Current Drive	I_{AMIOUT}	-	-	20	mA
AMI Output *High* Voltage Output Current = 20mA	VOH AMI	VDD - 0.16	-	-	V
AMI Output *Low* Voltage Output Current = 20mA	$V_{OL\ AMI}$	-	-	0.16	V
Nominal Test Load Impedance	R_{TEST}	-	110	-	Ω
"Mark" Amplitude After Transformer	V_{MARK}	0.9	1.0	1.1	V
"Space" Amplitude After Transformer	V_{SPACE}	- 0.1	0	0.1	V

Figure 17 Signal Structure of 64 kHz/8 kHz Central Clock Interface)



Note : For inputs this waveform would be A.C. coupled to the I1, I2 inputs.
For outputs this would be the waveform after a suitable output transformer (also see G.703[6]).

Figure 18 AMI Input and Output Signal Levels

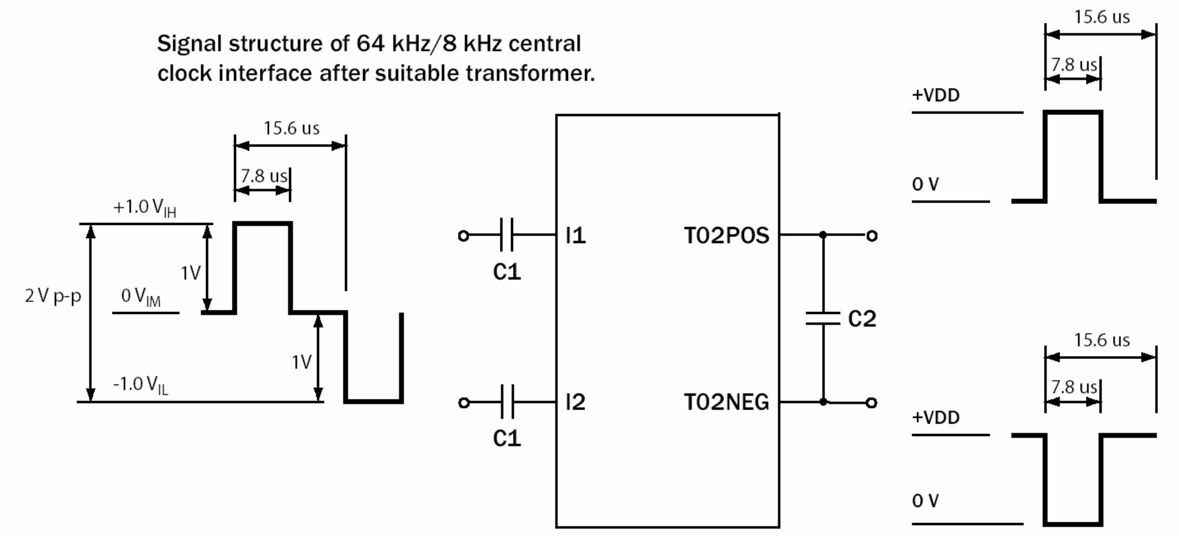
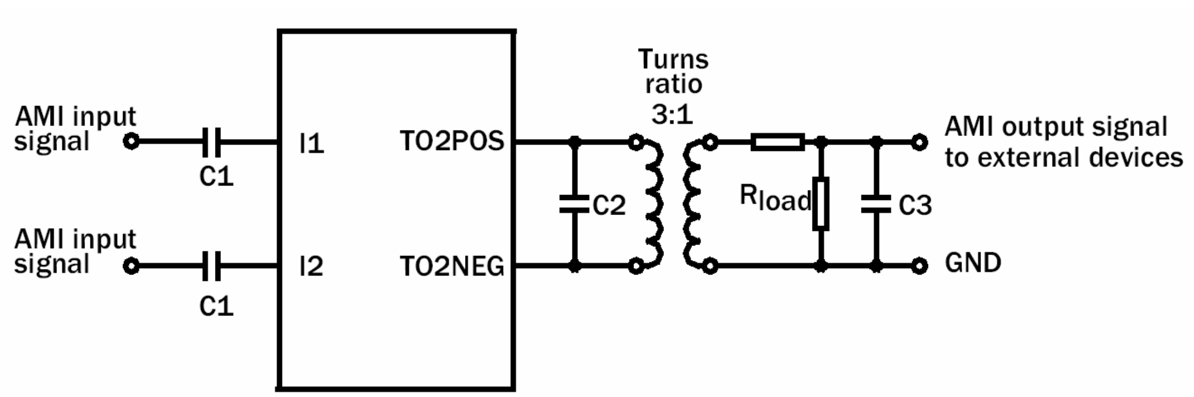


Figure 19 Recommended Line Termination for AMI Output/Output Ports

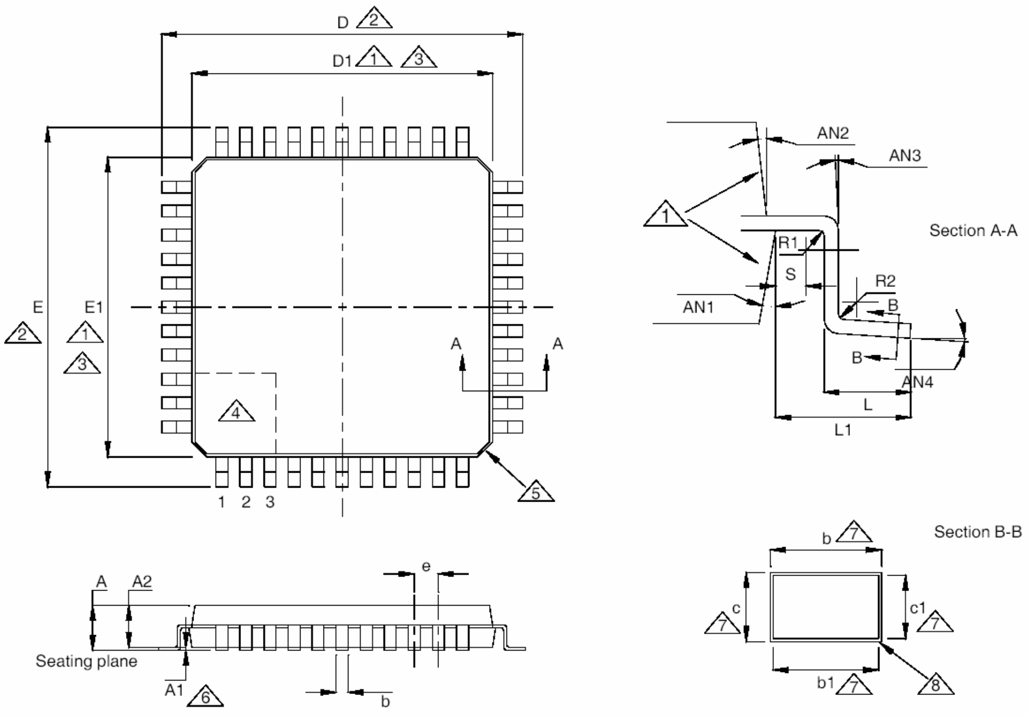


The AMI inputs I1 and I2 should be connected to the external AMI clock source by 470 nF coupling capacitor C1.

The AMI differential output TO2POS/TO2NEG should be coupled to a line transformer with a turns ratio of 3:1. Components C2 = 470 pF and C3 = 2 nF. If a transformer with a turns ratio of 1:1 is used, a 3:1 ratio potential divider R_{load} must be used to achieve the required 1 V pk-pk voltage level for the positive and negative pulses.

Package Information

Figure 20 LQFP Package



Notes

1. The top package body may be smaller than the bottom package body by as much as 0.15 mm.
2. To be determined at seating plane.
3. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Details of pin 1 identifier are optional but will be located within the zone indicated.
5. Exact shape of corners can vary.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
8. Shows plating.

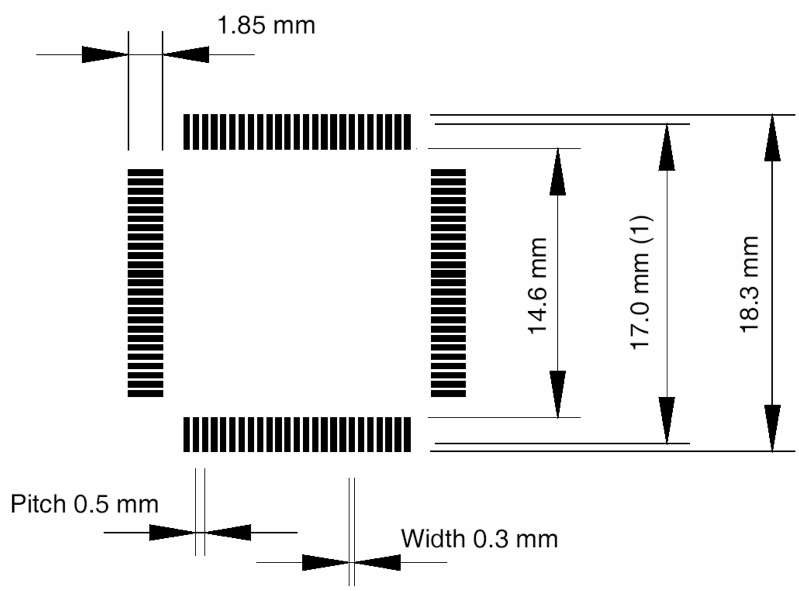
Table 30 100 Pin LQFP Package Dimension Data (for use with Figure 20)

100 LQFP Package Dimensions in mm	D/E	D1/ E1	A	A1	A2	e	AN1	AN2	AN3	AN4	R1	R2	L	L1	S	b	b1	c	c1
Min.	-	-	1.40	0.05	1.35	-	11o	11o	0o	0o	0.08	0.08	0.45	-	0.20	0.17	0.17	0.09	0.09
Nom.	16.00	14.00	1.50	0.10	1.40	0.50	12o	12o	-	3.5o	-	-	0.60	1.00 (ref)	-	0.22	0.20	-	-
Max.	-	-	1.60	0.15	1.45	-	13o	13o	-	7o	-	0.20	0.75	-	-	0.27	0.23	0.20	0.16

Thermal Conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Figure 21 Typical 100 Pin LQFP Footprint



Notes :

(i) Solderable to this limit.

(ii) Square package - dimensions apply in both X and Y directions.

(iii) Typical example. The user is responsible for ensuring compatibility with PCB manufacturing process, etc.

Simplified Application Schematic

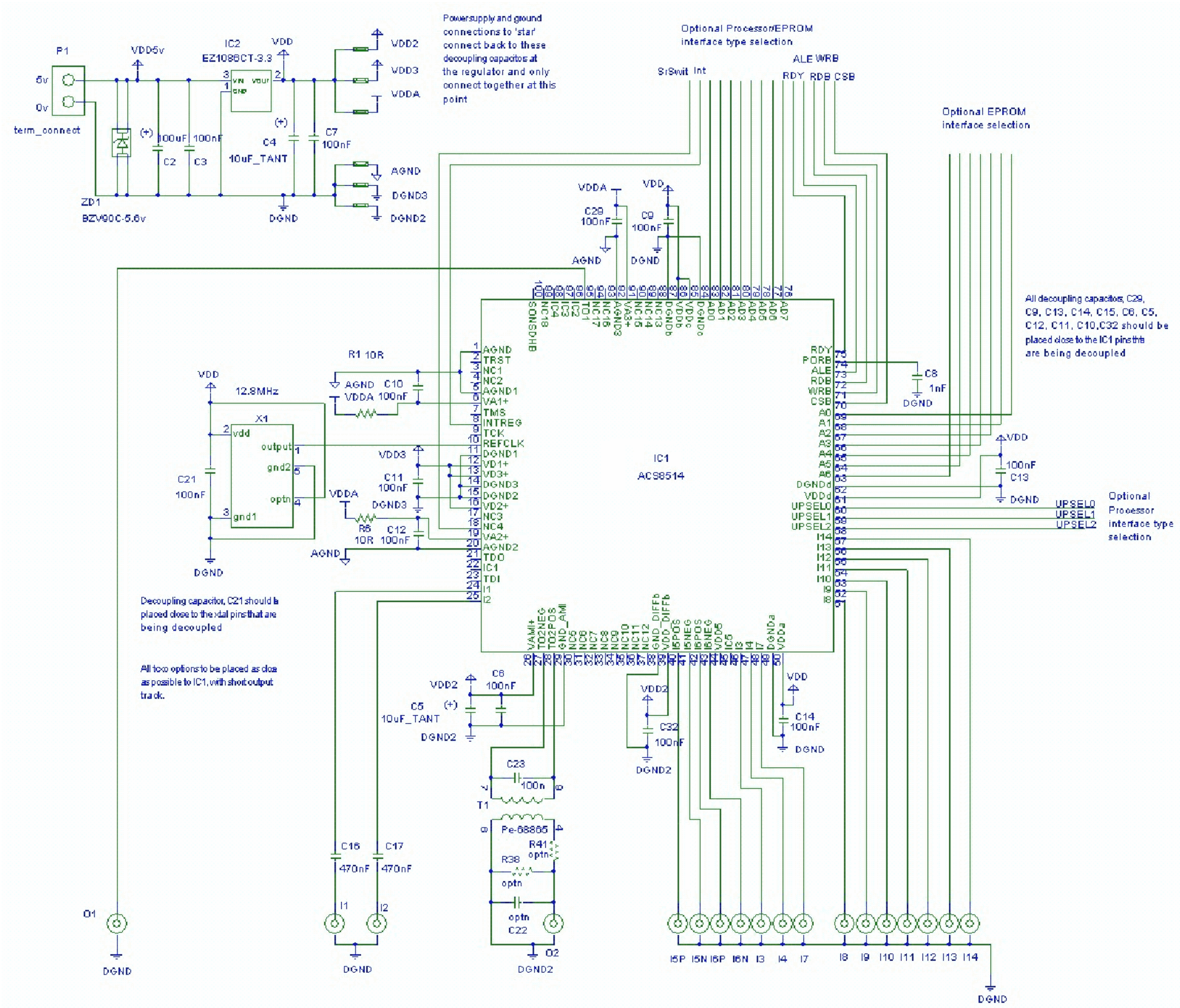


Figure 22 Simplified, ACS8514 circuit diagram.
The wiring configuration is very similar to an ACS8520/30 to which it is partnered and generally wired to, in parallel.

Abbreviations

AMI	Alternate Mark Inversion
APLL	Analogue Phase Locked Loop
BITS	Building Integrated Timing Supply
DFS	Digital Frequency Synthesis
DPLL	Digital Phase Locked Loop
DS1	1544 kb/s interface rate
DTO	Discrete Time Oscillator
E1	2048 kb/s interface rate
I/O	Input - Output
LOF	Loss of Frame Alignment
LOS	Loss Of Signal
LQFP	Low profile Quad Flat Pack
LVDS	Low Voltage Differential Signal
MTIE	Maximum Time Interval Error
NE	Network Element
OCXO	Oven Controlled Crystal Oscillator
PBO	Phase Build-out
PDH	Plesiochronous Digital Hierarchy
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
ppb	parts per billion
ppm	parts per million
pk-pk	peak-to-peak
R/W	Read/Write
rms	root-mean-square
RO	Read Only
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TDEV	Time Deviation
TCXO	Temperature Compensated Crystal Oscillator
UI	Unit Interval
WEEE	Waste Electrical and Electronic Equipment (directive)

References

[1] ANSI T1 1.101-1999 (1999)
Synchronization Interface Standard

[2] AT & T 62411 (12/1990)
ACCUNET® T1.5 Service description and Interface Specification

[3] ETSI ETS 300 462-3, (01/1997)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3: The control of jitter and wander within synchronization networks

[4] ETSI ETS 300 462-5 (09/1996)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment

[5] IEEE 1149.1 (1990)
Standard Test Access Port and Boundary-Scan Architecture

[6] ITU-T G.703 (10/1998)
Physical/electrical characteristics of hierarchical digital interfaces

[7] ITU-T G.736 (03/1993)
Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s

[8] ITU-T G.742 (1988)
Second order digital multiplex equipment operating at 8448 kbit/s, and using positive justification

[9] ITU-T G.783 (10/2000)
Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks

[10] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[11] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[12] ITU-T G.822 (11/1988)
Controlled slip rate objectives on an international digital connection

[13] ITU-T G.823 (03/2000)
The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

[14] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[15] ITU-T G.825 (03/2000)
The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH)

[16] ITU-T K.41 (05/1998)
Resistability of internal interfaces of telecommunication centres to surge overvoltages

[17] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[18] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[19] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

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Notes

Revision Status/History

The Revision Status, as shown in top right corner of the datasheet, may be TARGET, PRELIMINARY, or FINAL, and refers to the status of the Device (not the datasheet), with the design cycle. TARGET status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design. The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is a FINAL release of the ACS8514 datasheet. Changes made for this document revision are given in Table 31.

Table 31 Revision History

Revision	Reference	Description of changes
1.00/April 2003	All Pages	Initial datasheet at Preliminary status. Refer to particular release for the changes made for that release.
1.01/May 2003	All Pages	General prerelease update for typo's & reviewer comments. ESD & Latchup section added & Application schematic
1.02/July 2003	Register 09, bit 6, reg 73, bit 6	Update to register operation description.
2.00/September 2003	All Pages	Update to Final status
3.00/April 2007	All Pages	Business group name change to Advanced Comms & Sensing.
	Front page, Abbreviations and References	Updated for RoHS and WEEE references.
	Back Page	Business group name change to Advanced Comms & Sensing. Added Lead (Pb) free ordering information

Ordering Information

Table 32 Parts List

Part Number	Description
ACS8514	Synchronous Equipment Timing Source Partner IC for 2nd T4 DPLL, Accurate Monitoring & Input Extender. Partners the ACS8520 & ACS8530 for use in SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) applications.
ACS8514T	Lead (Pb)-free packaged version of ACS8525; RoHS and WEEE compliant.

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