19-3920; Rev 0; 12/05

MAX12527/MAX12528/MAX12529/ MAX12557/MAX12558/MAX12559 Evaluation Kits

Evaluate: MAX12527/28/29/57/58/59

General Description

The MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 evaluation kits (EV kits) are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of this family of 12-bit and 14-bit, dual analog-to-digital converters (ADCs). These ADCs accept differential analog input signals. The EV kits generate these signals from user-provided single-ended input sources. The digital outputs produced by the ADCs can be easily sampled with a user-provided high-speed logic analyzer or data-acquisition system. The EV kits operate from 2.0V and 3.3V power supplies.

Part Selection Table

PART	SAMPLING RATE (Msps)	RESOLUTION (Bits)
MAX12559ETK	96	14
MAX12558ETK	80	14
MAX12557ETK	65	14
MAX12529ETK	96	12
MAX12528ETK	80	12
MAX12527ETK	65	12

Features

- ♦ **Low-Voltage and Low-Power Operation**
- ♦ **On-Board Clock-Shaping Circuitry Option**
- ♦ **On-Board Output Drivers**
- ♦ **Fully Assembled and Tested**

Ordering Information

PART	TEMP RANGE*	IC PACKAGE
MAX12527EVKIT	0°C to +70°C	68 TQFN-EP**
MAX12528EVKIT	0°C to +70°C	68 TQFN-EP**
MAX12529EVKIT	0°C to +70°C	68 TQFN-EP**
MAX12557EVKIT	0°C to +70°C	68 TQFN-EP**
MAX12558EVKIT	0°C to +70°C	68 TQFN-EP**
MAX12559EVKIT	0°C to +70°C	68 TQFN-EP**

**EV kit PC board temperature range only.*

***EP = Exposed paddle.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C4	0	Not installed (0603)
C5, C6, C11, C13, C14, C16, C17, C28–C32, C45, C46, C57–C60, C62–C65	22	0.1µF ±20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M
C7–C10	4	5.6pF ±0.5pF, 50V C0G ceramic capacitors (0402) TDK C1005C0G1H5R6D
C12, C21–C27	8	4.7µF ±20%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J475M
C15, C18 C19, C20	4	0.1µF ±20%, 6.3V X5R ceramic capacitors (0201) TDK C0603X5R0J104M

DESIGNATION	QTY	DESCRIPTION
C33–C38, C47, C53	8	220µF ±20%, 6.3V tantalum capacitors (C case) AVX TPSC227M006R0250
C39, C40, C41, C55, C61, C66	6	10µF ±20%, 6.3V X5R ceramic capacitors (0805) TDK C2012X5R0J106M
C42, C43, C44, C56	4	1.0µF ±20%, 10V X5R ceramic capacitors (0603) TDK C1608X5R1A105M
C51, C52	2	0.01µF ±5%, 25V C0G ceramic capacitors (0603) TDK C1608C0G1E103J
C67	1	1.0µF ±20%, 6.3V X5R ceramic capacitor (0402) TDK C1005X5R0J105M

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
D1	1	Dual Schottky diode (SOT23) Central Semiconductor CMPD6263S Vishay BAS70-04 Diodes Inc. BAS70-04
J1, J2, J7	3	SMA PC mount connectors
J3, J4, J8	3	2-pin headers
J5, J6	2	Dual-row, 40-pin headers (2 x 20)
JU1–JU6	6	3-pin headers
L1–L4	4	EMI filters Murata NFM41PC204F1H3B
R1–R8, R13–R16, R21–R32, R37, R40–R45	0	Not installed (0603)
R9–R12	4	75Ω ±0.5% resistors (0603)
R17–R20	4	110Ω ±0.5% resistors (0603)
R33–R36	0	Not installed (0402)
R38, R39	2	49.9Ω ±1% resistors (0603)
R46, R47	2	100Ω ±1% resistors (0603)
R48	1	10kΩ potentiometer
R49–R52	4	24.9Ω ±0.5% resistors (0402)

DESIGNATION	QTY	DESCRIPTION
RA1–RA8	8	220Ω ±5% resistor arrays Panasonic EXB-2HV-221J
T1–T4	4	1:1 RF transformers Mini-Circuits ADT1-1WT
T5	1	1:2 RF transformer Coilcraft TTWB-2-B
TP1–TP6	6	Test points
U1	1	See the *EV Kit Specific Component List*
U2, U3	2	Low-voltage 16-bit registers (48-pin TSSOP) Pericom PI74ALVTC16374 or Texas Instruments SN74AVC16374DGGR
U4	1	TinyLogic ULP-A buffer (SC70-5) Fairchild NC7SV125P5
U5	1	TinyLogic ULP-A inverter (SC70-6) Fairchild NC7WV04P6
None	6	Shunts
None	1	MAX12527/MAX12528/MAX12529/ MAX12557/MAX12558/MAX12559 PC board

EV Kit Specific Component List

EV KIT PART NUMBER	REFERENCE DESIGNATOR	DESCRIPTION
MAX12527EVKIT	U1	Maxim MAX12527ETK (68-pin thin QFN, 10mm x 10mm x 0.8mm)
MAX12528EVKIT		Maxim MAX12528ETK (68-pin thin QFN, 10mm x 10mm x 0.8mm)
MAX12529EVKIT		Maxim MAX12529ETK (68-pin thin QFN, 10mm x 10mm x 0.8mm)
MAX12557EVKIT		Maxim MAX12557ETK (68-pin thin QFN, 10mm x 10mm x 0.8mm)
MAX12558EVKIT		Maxim MAX12558ETK (68-pin thin QFN, 10mm x 10mm x 0.8mm)
MAX12559EVKIT		Maxim MAX12559ETK (68-pin thin QFN, 10mm x 10mm x 0.8mm)

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
Central Semiconductor	631-435-1110	631-435-1824	www.centralsemi.com
Coilcraft	847-639-6400	847-639-1469	www.coilcraft.com
Diodes Inc.	805-446-4800	805-446-4850	www.diodes.com
Fairchild	888-522-5372	—	www.fairchildsemi.com
Murata	770-436-1300	770-436-3030	www.murata.com
Panasonic	714-373-7366	714-737-7323	www.panasonic.com
Pericom	800-435-2336	408-435-1100	www.pericom.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Texas Instruments	972-644-5580	214-480-7800	www.ti.com

Note: *Indicate that you are using the MAX12527, MAX12528, MAX12529, MAX12557, MAX12558, and MAX12559 when contacting these component suppliers.*

Quick Start

Recommended Equipment

- DC power supplies:
  - Analog (VDD) 3.3V, 500mA
  - Digital (OVDD) 2.0V, 50mA
  - Buffers (VLOGIC) 2.0V, 100mA
- Signal generator with low phase noise and low jitter for clock input signal (e.g., HP/Agilent 8644B)
- Two signal generators with low phase noise for analog signal inputs (e.g., HP/Agilent 8644B)
- Logic analyzer or data-acquisition system (e.g., HP/Agilent 16500C)
- Narrow-band analog bandpass filters (e.g., Allen Avionics, K&L Microwave) for input signals and clock signal
- Digital multimeter

Procedure

The EV kit is a fully assembled and tested printed circuit (PC) board. Follow the steps below to verify board operation. **Do not turn on power supplies or enable signal generators until all connections are completed.**

1) Verify that shunts are installed in the following locations:
   JU1 (2-3) → Independent reference mode
   JU2 (2-3) → ADC active (not in power-down mode)
   JU3 (2-3) → Outputs in two's-complement format
   JU4 (1-2) → Differential clock input
   JU5 (2-3) → No clock division
   JU6 (2-3) → No clock division
2) Connect the clock signal generator to the input of the clock bandpass filter.
3) Connect the output of the clock bandpass filter to the SMA connector labeled J7.
4) Connect the analog input signal generators to the inputs of the desired analog bandpass filters. For best results, connect the bandpass filter directly to the SMA connector and forego any cables in between.
5) Connect the output of the analog bandpass filters to the SMA connectors labeled J1 and J2. The analog input signals can be monitored at J3 and J4. Eliminate cables between bandpass filter outputs and SMA connectors. If cables must be used, they should be as short as possible. Add a 3dB to 6dB attenuator between bandpass filter and SMA connectors to control undesired distortion components induced by the signal generator.
6) Connect the logic analyzer to headers J5 and J6 to collect digitized data from channels A and B. See the *Output Bit Locations* section in this document for header connections.
7) Connect a 3.3V, 500mA power supply to VDD and connect its ground terminal to the GND pad.
8) Connect a 2.0V, 50mA power supply to OVDD and connect its ground terminal to the GND pad.
9) Connect a 2.0V, 100mA power supply to VLOGIC and connect its ground terminal to the GND pad.
10) Short the VCLK pad to the corresponding GND pad. **Note:** The VCLK supply is only required when the data converter is operating in single-ended clock mode. See the *Configuring the EV Kit for Single-Ended Clock Operation* section in this document for further details.

11) Turn on all the power supplies.

12) Enable the signal generators.

13) Set the clock signal generator to the desired clock frequency. See the *Part Selection Table* for the appropriate frequency settings for each EV kit. The amplitude of the generator should be sufficient to produce a 16dBm signal at the SMA input of the EV kit. Insertion losses due to the series-connected filter (step 2) and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude.

14) Set the analog input signal generators to output the desired test frequency. The amplitude of the generator should produce a signal that is no larger than 7.5dBm as measured at the SMA input of the EV kit. Insertion losses due to the series-connected filter (step 5) and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude. Also account for the attenuation from the 3dB to 6dB attenuator.

15) All signal generators should be phase-locked to each other.

16) Enable the logic analyzer.

17) Collect data using the logic analyzer.

Detailed Description

The EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX12527, MAX12528, MAX12529, MAX12557, MAX12558, or MAX12559.

The ADCs accept differential input signals; however, on-board transformers (T1–T4) convert a readily available single-ended source output to the required differential signal. The input signals of the ADC can be measured using a differential oscilloscope probe at headers J3 and J4.

Output drivers (U2 and U3) buffer the output signals of the data converter. The digital outputs of the EV kit are accessible at headers J5 and J6.

The EV kits are designed as a four-layer PC board to optimize the performance of this family of ADCs. Separate analog, digital, clock, and buffer power planes minimize noise coupling between analog and digital signals. 100Ω differential microstrip transmission lines are used for analog and clock inputs. 50Ω microstrip transmission lines are used for all digital outputs. The trace lengths of the 100Ω differential input lines are matched to within a few thousandths of an inch to minimize layout-dependent input-signal skew.

Power Supplies

For best performance, the EV kits require separate analog, digital, clock, and buffer power-supply sources. Individual 3.3V and 2.0V power supplies are recommended to power the analog (VDD) and digital (OVDD) portions of the converter. A separate 2.0V power supply (VLOGIC) is used to power the output buffers (U2, U3) of the EV kit. The on-board clock circuitry (VCLK) is powered by a 3.3V power supply. The VCLK supply is only required when the ADC is operating in single-ended clock mode. See the *Configuring the EV Kit for Single-Ended Clock Operation* section for further details.

Converter Power-Down

The MAX12527, MAX12528, MAX12529, MAX12557, MAX12558, and MAX12559 each feature an active-high global device power-down pin. Jumper JU2 controls this feature. See Table 1 for shunt positions.

Table 1. Power-Down Shunt Settings (JU2)

SHUNT POSITION	PD PIN	DESCRIPTION
1-2	OVDD	ADC powered down
2-3*	GND	ADC active (normal operation)

**Default configuration: JU2 (2-3).*

Clock

Additionally, the data converter allows for either differential or single-ended signals to drive the clock inputs. The MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV kits support both methods.

In single-ended operation, the clock signal is applied to the ADC through a buffer (U5). In differential mode, an on-board transformer converts a user-provided single-ended analog input and generates a differential analog signal, which is then applied to the ADC's input pins.

Jumper JU4 controls the ADC clock input. See Table 2 for jumper configuration.

Table 2. Clock Selection Shunt Settings (JU4)

SHUNT POSITION	DIFFCLK/$\overline{\text{SECLK}}$ PIN	DESCRIPTION
1-2*	OVDD	**Differential clock mode.**
2-3	GND	**Single-ended clock mode.** See the *Configuring the EV Kit for Single-Ended Clock Operation* section for further details.

**Default configuration: JU4 (1-2).*

Configuring the EV Kits for Single-Ended Clock Operation

To configure the MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV kits for single-ended clock operation, the following modifications must be made to the clock circuit:

1) Cut the trace at locations R41, R43, and R44.
2) Install 0Ω resistors at locations R40, R42, and R45.
3) Install a 49.9Ω ±1% resistor at location R37.
4) Connect a 3.3V power supply to VCLK (needs to be capable of sourcing up to 10mA output current). Connect the ground terminal of this supply to GND.

In single-ended clock configuration, potentiometer R48 can be utilized to control the duty cycle of the clock input signal. Measure the clock input at J8 and adjust R48 until the desired duty cycle is achieved.

Clock-Divider Control

The MAX12527, MAX12528, MAX12529, MAX12557, MAX12558, and MAX12559 each feature internal divide-by-2/divide-by-4 clock-divider circuitry (DIV2, DIV4). Jumpers JU5 and JU6 control this circuitry. Refer to the individual ADC data sheets for a detailed explanation of the internal clock divider. See Table 3 for jumper configuration.

Table 3. Clock-Divider Shunt Settings (JU5, JU6)

SHUNT POSITION		PIN CONNECTION		DESCRIPTION
JU5	JU6	DIV2	DIV4	
2-3*	2-3*	GND	GND	Normal clock mode
1-2	2-3	OVDD	GND	Divide-by-2 clock mode (DIV2)
2-3	1-2	GND	OVDD	Divide-by-4 clock mode (DIV4)
1-2	1-2	OVDD	OVDD	**INVALID**

**Default configuration: JU5 (2-3), JU6 (2-3).*

Input Signal

Although this family of ADCs accepts differential analog input signals, the EV kit only requires single-ended analog input signals, with amplitudes less than 7.5dBm. Insertion losses due to a series-connected filter and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude. On-board transformers (T1–T4) convert the single-ended analog input signals and generate the recommended differential analog signals at the ADCs' differential input pins.

Optimizing the Analog Input Network for Different Input Frequencies

The EV kits are designed for excellent AC performance across a broad 3MHz to 400MHz input frequency range. The design can be further optimized by adjusting components C7–C10 and R49–R52. See Table 4 for the appropriate component values for specific input frequency ranges.

Table 4. Component Selection for Optimized AC Performance

INPUT FREQUENCY RANGE (MHz)	C7–C10 COMPONENT VALUES (pF)	R49–R52 COMPONENT VALUES (Ω)
3 to 400*	5.6	25
< 10	12 to 22	0
10 to 125	12	25 to 50
> 125	5.6 to 12	0

**Default EV kit configuration.*

Reference

The MAX12527, MAX12528, MAX12529, MAX12557, MAX12558, and MAX12559 feature numerous reference operation modes. The default EV kit configuration connects the ADC's internal 2.048V reference output to the reference input. In this case, the converter generates the REFN, REFP, and COM voltages from this input (refer to the individual ADC's data sheet for a more detailed explanation).

To apply a user-supplied reference, cut the trace at location R33 and connect the desired external reference to the REFIN pad. Alternatively, the EV kit can be configured to use a divided internal reference value. If the desired reference voltage is less than 2.048V, cut the trace at location R33 and install resistors in locations R33 and R34. Calculate the resistor values from the equations below:

$$R34 = \frac{V_{REF}}{V_{REFOUT}} \times R_T$$

$$R33 = R_T - R34$$

where:

V_{REF} = desired reference voltage

V_{REFOUT} = ADC's internal reference voltage of 2.048V

R_T = ADC's minimum reference resistance ≈ 10kΩ

Shared Reference Mode

To maximize isolation between the two input channels, the MAX12527, MAX12528, MAX12529, MAX12557, MAX12558, and MAX12559 feature two independent references. To improve channel matching this family of ADCs provides a mode where both input channels share the same reference. Jumper JU1 controls this shared reference feature. See Table 5 for the desired jumper configuration.

Table 5. Shared Reference Shunt Settings (JU1)

SHUNT POSITION	SHREF PIN	DESCRIPTION
1-2	OVDD	Shared reference mode. Install 0Ω resistors at locations R35 and R36.
2-3*	GND	Independent reference mode. Remove any component at locations R35 and R36.

**Default configuration: JU1 (2-3).*

Alternative Reference Mode

The MAX12527, MAX12528, MAX12529, MAX12557, MAX12558, and MAX12559 derive their REFP, REFN, and COM voltages from the REFIN input. To override these derived voltages, follow the board modifications given below.

1) Cut the trace at location R33.
2) Remove resistor R34 (not installed by default).
3) Connect the REFIN pad to GND.
4) Apply the desired voltages to test points TP1–TP6.

See Table 6 for a detailed description of test point connections.

Table 6. Reference Test Point Connections

TEST POINT	CONNECTION	DESCRIPTION
TP1	COMA	Common-mode voltage for channel A.
TP2	COMB	Common-mode voltage for channel B.
TP3	REFPA	Positive voltage reference terminal for channel A.
TP4	REFNA	Negative voltage reference terminal for channel A.
TP5	REFPB	Positive voltage reference terminal for channel B.
TP6	REFNB	Negative voltage reference terminal for channel B.

Note: *Refer to the respective ADC data sheet for REFP, REFN, and COM voltage ranges.*

Output Signal

The MAX12527, MAX12528, and MAX12529 feature two 12-bit, parallel, CMOS-compatible digital outputs that transmit the converted analog input signals. The higher-resolution MAX12557, MAX12558, and MAX12559 feature two 14-bit, parallel, CMOS-compatible digital outputs that transmit the converted analog input signals. Each set of 12-bit or 14-bit digital outputs also includes a clock (CLK) bit and overrange (DORA/B) bit to accommodate data synchronization and error detection. See the *Output Bit Locations* section for more details on how to configure these 12-bit and 14-bit converter outputs.

Output Format

Set the digital output coding to either two's-complement or Gray code, by configuring jumper JU3. See Table 7 for the jumper configuration.

Table 7. Output Format Shunt Settings (JU3)

SHUNT POSITION	G/$\overline{T}$ Pin	DESCRIPTION
1-2	OVDD	**Gray code selected.** Digital output format is Gray code.
2-3*	GND	**Two's complement selected.** Digital output format is two's complement.

**Default configuration: JU3 (2-3).*

Output Bit Locations

Two drivers (U2 and U3) buffer the digital outputs of the individual ADCs. These drivers can drive large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to 40-pin headers J5 and J6. See Table 8 (14-bit ADCs) and Table 9 (12-bit ADCs) for bit locations of headers J5 and J6.

Note: Silkscreen markings on the EV kit PC board indicate pin markings for the MAX12557, MAX12558, and MAX12559. These pin markings are not valid for the MAX12527, MAX12528, or MAX12529. Use the connections outlined in Table 9.

Table 8. Output Bit Locations (MAX12557, MAX12558, MAX12559—14-Bit, Dual ADCs)

SIGNAL	CHANNEL		DESCRIPTION
	A	B	
D0	J5-37	J6-37	Data Bit 0 (LSB)
D1	J5-35	J6-35	Data Bit 1
D2	J5-33	J6-33	Data Bit 2
D3	J5-31	J6-31	Data Bit 3
D4	J5-29	J6-29	Data Bit 4
D5	J5-27	J6-27	Data Bit 5
D6	J5-25	J6-25	Data Bit 6
D7	J5-23	J6-23	Data Bit 7
D8	J5-21	J6-21	Data Bit 8
D9	J5-19	J6-19	Data Bit 9
D10	J5-17	J6-17	Data Bit 10
D11	J5-15	J6-15	Data Bit 11
D12	J5-13	J6-13	Data Bit 12
D13	J5-11	J6-11	Data Bit 13 (MSB)
DOR	J5-9	J6-9	Over Range Bit
CLK	J5-3	J6-3	Clock Bit

Note: *Pins 1, 2, 5, 6, 39, and 40 of J5 and pins 1, 2, 5, 6, 7, 39, and 40 of J6 are open. All other pins that are not listed in Table 8 are connected to GND.*

Table 9. Output Bit Locations (MAX12527, MAX12528, MAX12529—12-Bit, Dual ADCs)

SIGNAL	CHANNEL		DESCRIPTION
	A	B	
N.C.	J5-37	J6-37	N.C.
N.C.	J5-35	J6-35	N.C.
D0	J5-33	J6-33	Data Bit 0 (LSB)
D1	J5-31	J6-31	Data Bit 1
D2	J5-29	J6-29	Data Bit 2
D3	J5-27	J6-27	Data Bit 3
D4	J5-25	J6-25	Data Bit 4
D5	J5-23	J6-23	Data Bit 5
D6	J5-21	J6-21	Data Bit 6
D7	J5-19	J6-19	Data Bit 7
D8	J5-17	J6-17	Data Bit 8
D9	J5-15	J6-15	Data Bit 9
D10	J5-13	J6-13	Data Bit 10
D11	J5-11	J6-11	Data Bit 11 (MSB)
DOR	J5-9	J6-9	Over Range Bit
CLK	J5-3	J6-3	Clock Bit

Note: *Pins 1, 2, 5, 6, 39, and 40 of J5 and pins 1, 2, 5, 6, 7, 39, and 40 of J6 are open. All other pins that are not listed in Table 9 are connected to GND.*

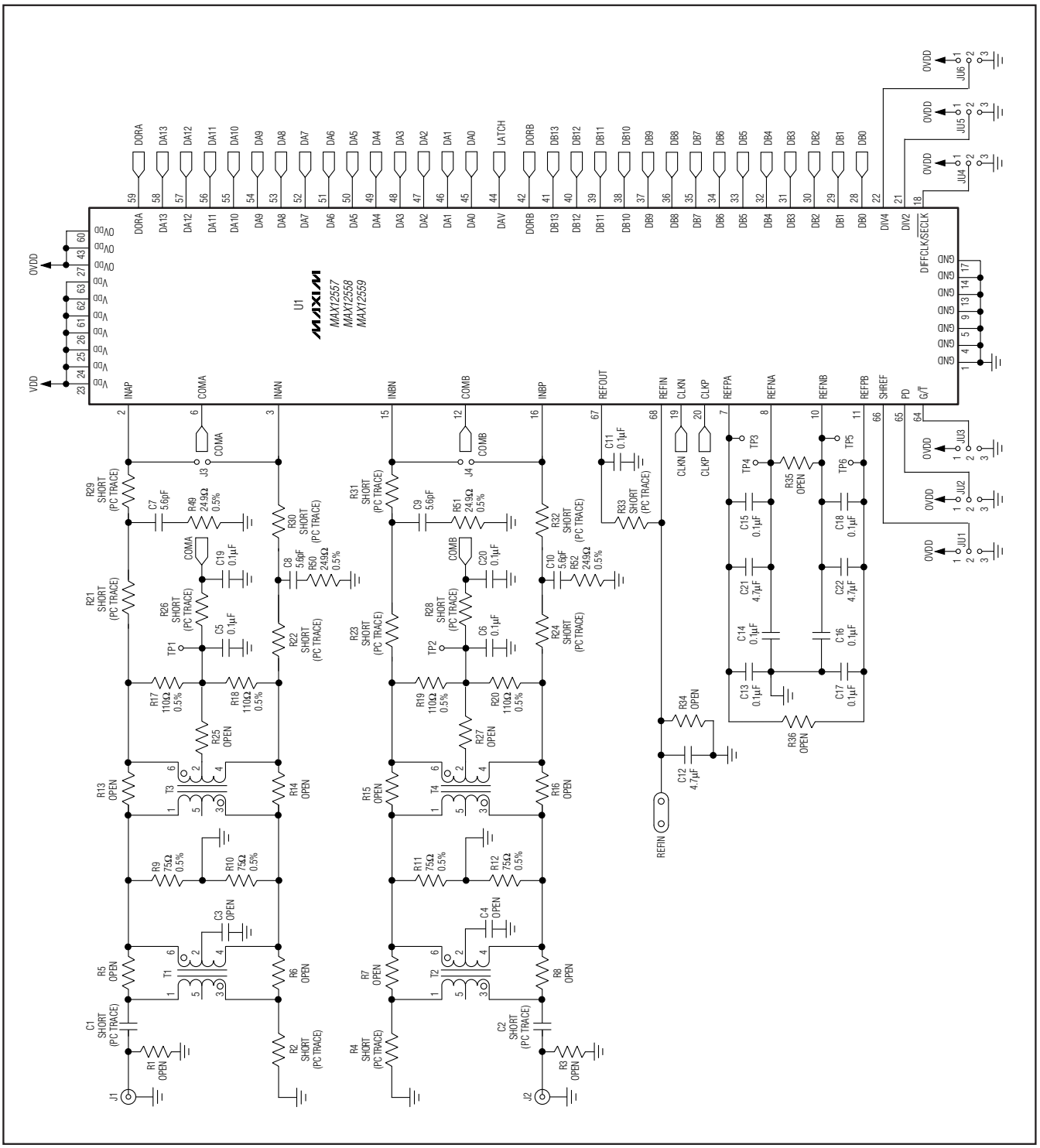

Figure 1. MAX12557/MAX12558/MAX12559 EV Kit Schematic (Sheet 1 of 4)

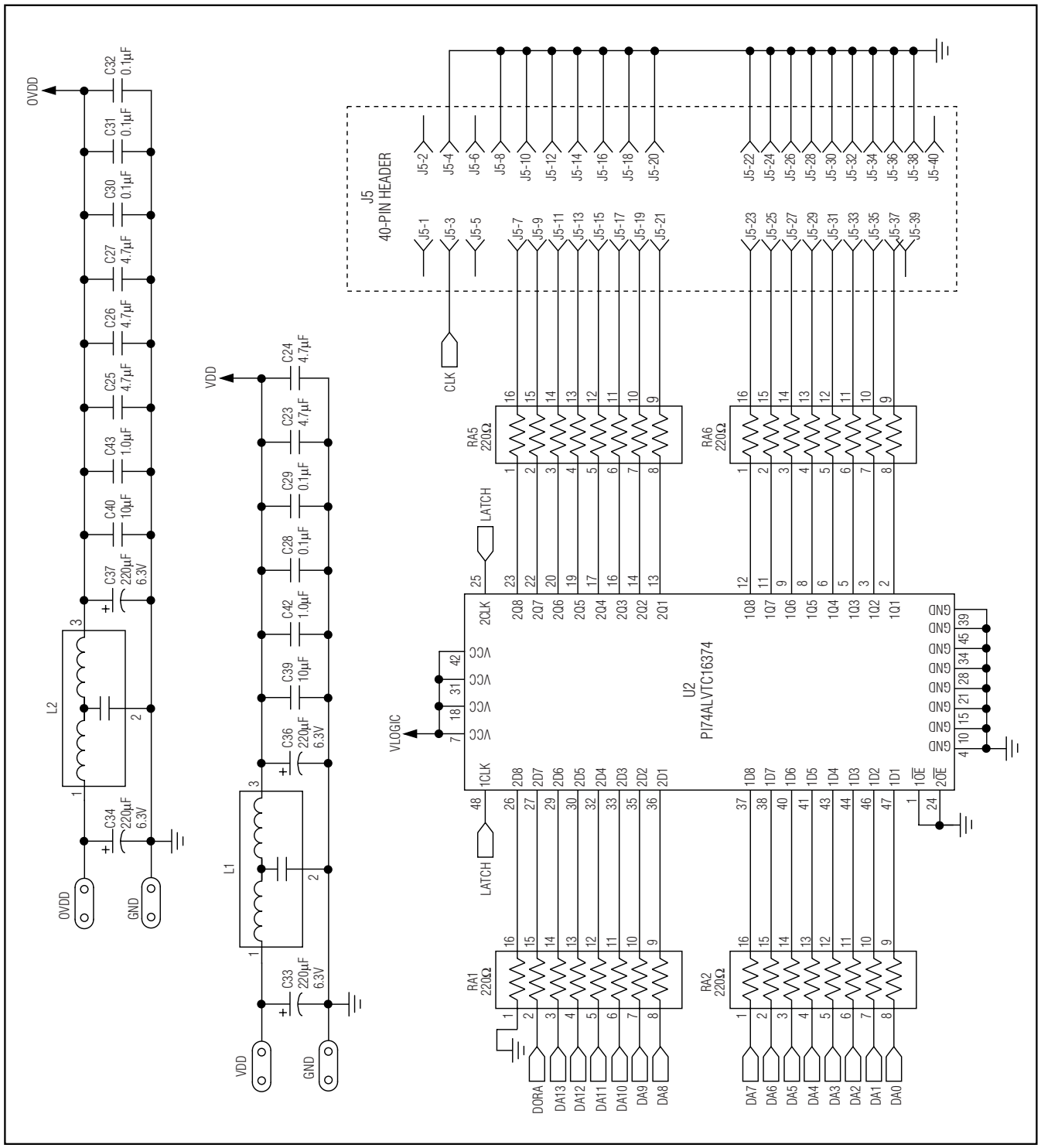

Figure 2. MAX12557/MAX12558/MAX12559 EV Kit Schematic (Sheet 2 of 4)

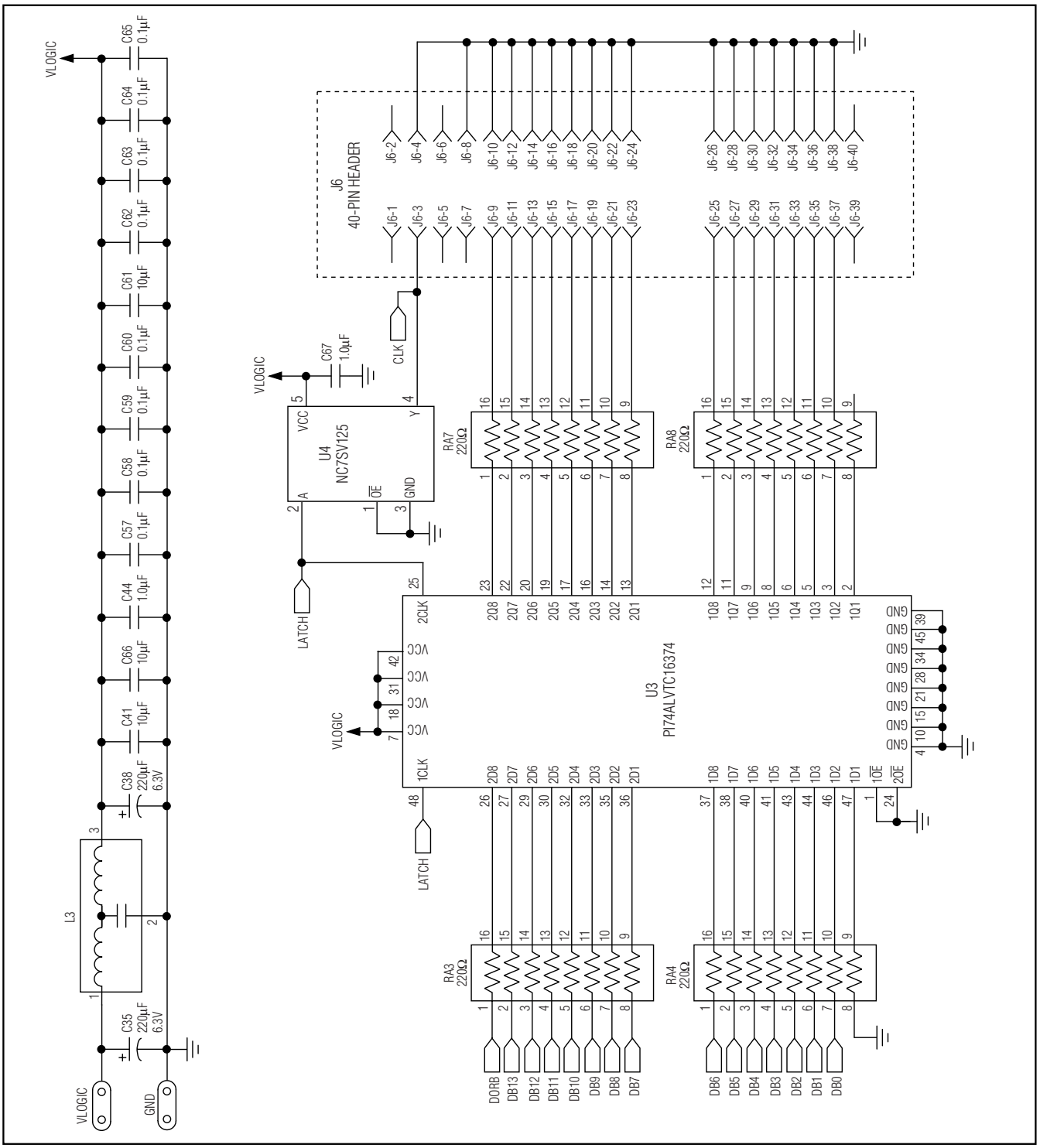

Figure 3. MAX12557/MAX12558/MAX12559 EV Kit Schematic (Sheet 3 of 4)

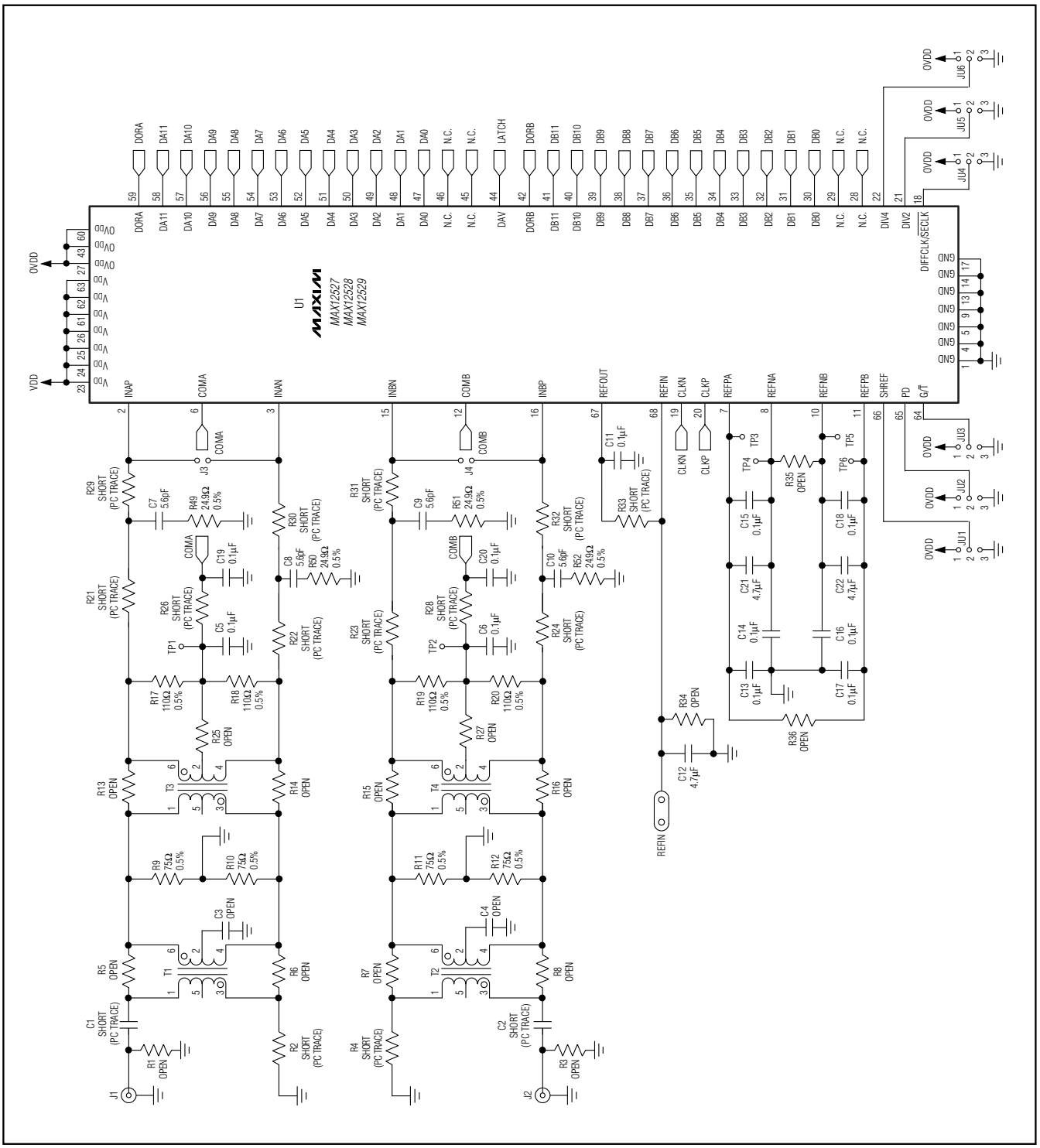

Figure 4. MAX12527/MAX12528/MAX12529 EV Kit Schematic (Sheet 1 of 4)

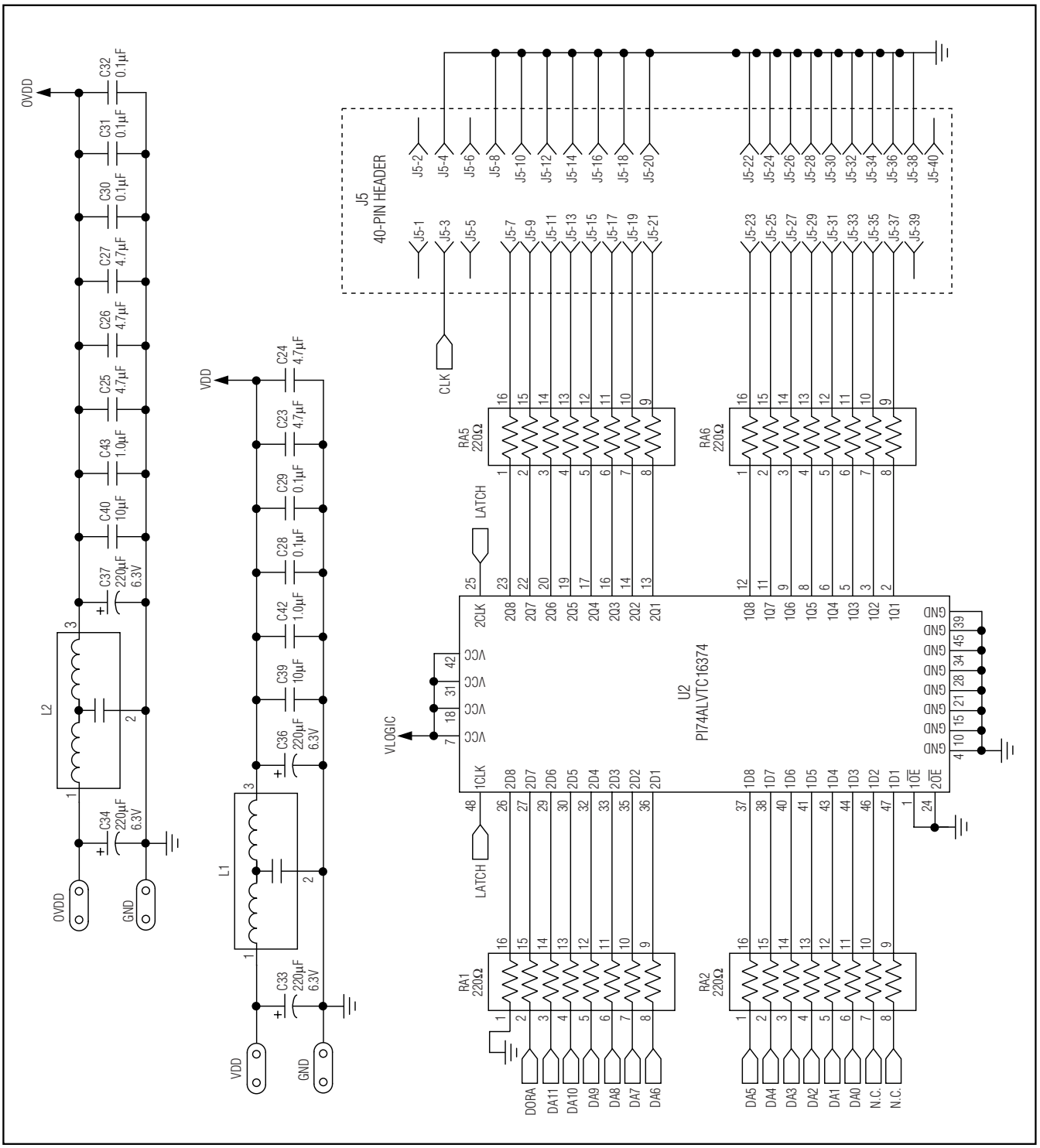

Figure 5. MAX12527/MAX12528/MAX12529 EV Kit Schematic (Sheet 2 of 4)

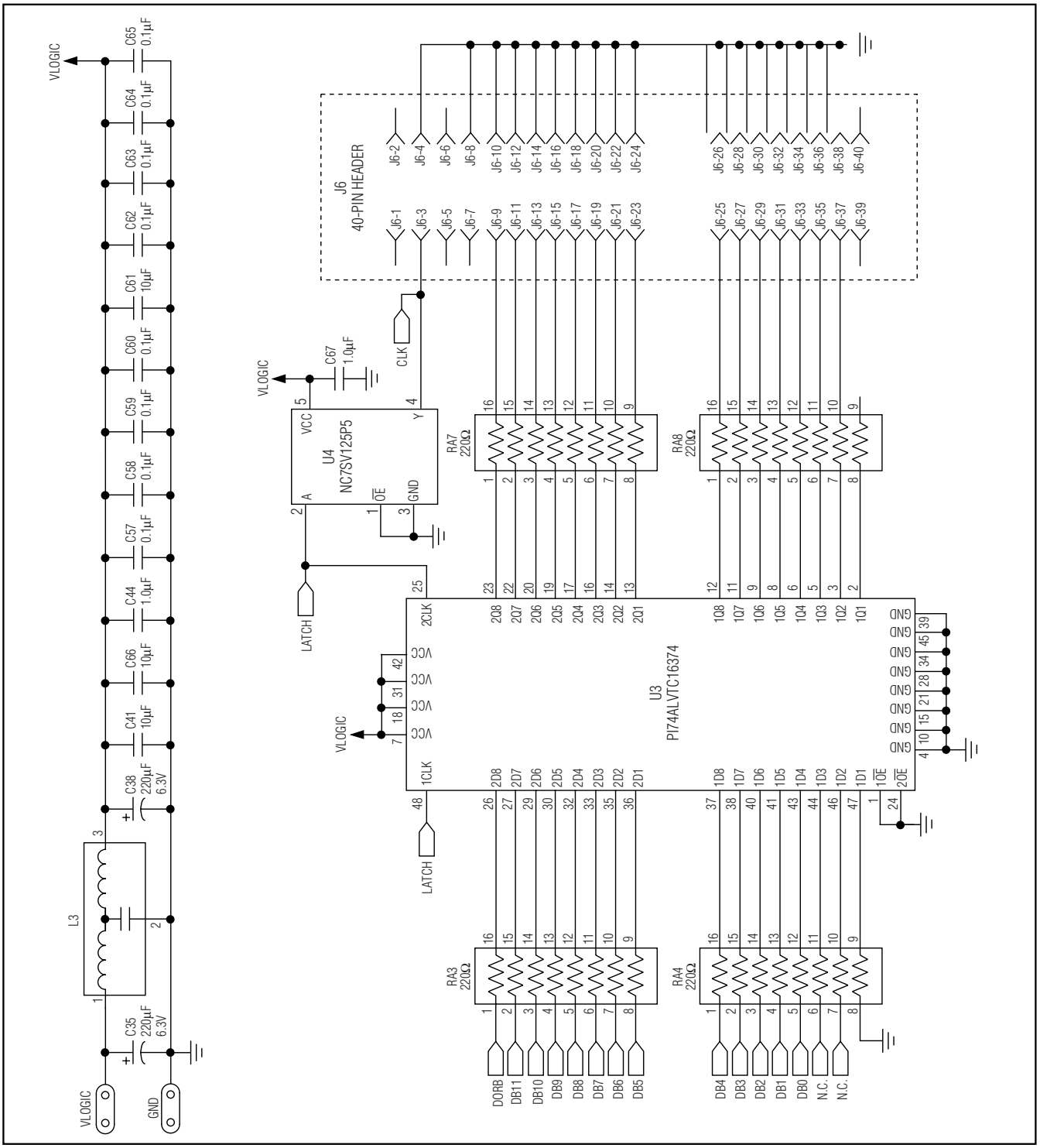

Figure 6. MAX12527/MAX12528/MAX12529 EV Kit Schematic (Sheet 3 of 4)

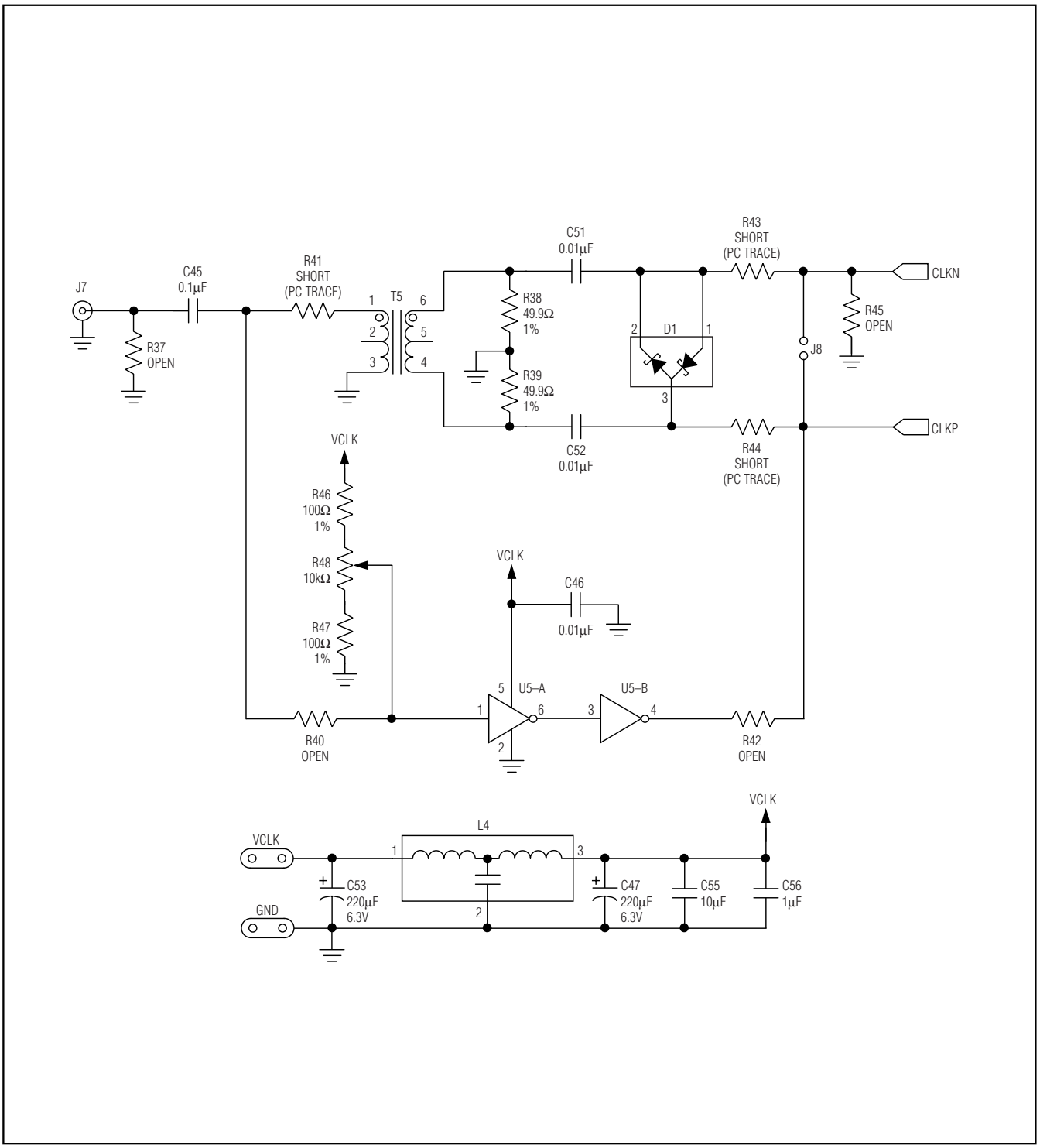

Figure 7. MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV Kit Schematic (Sheet 4 of 4)

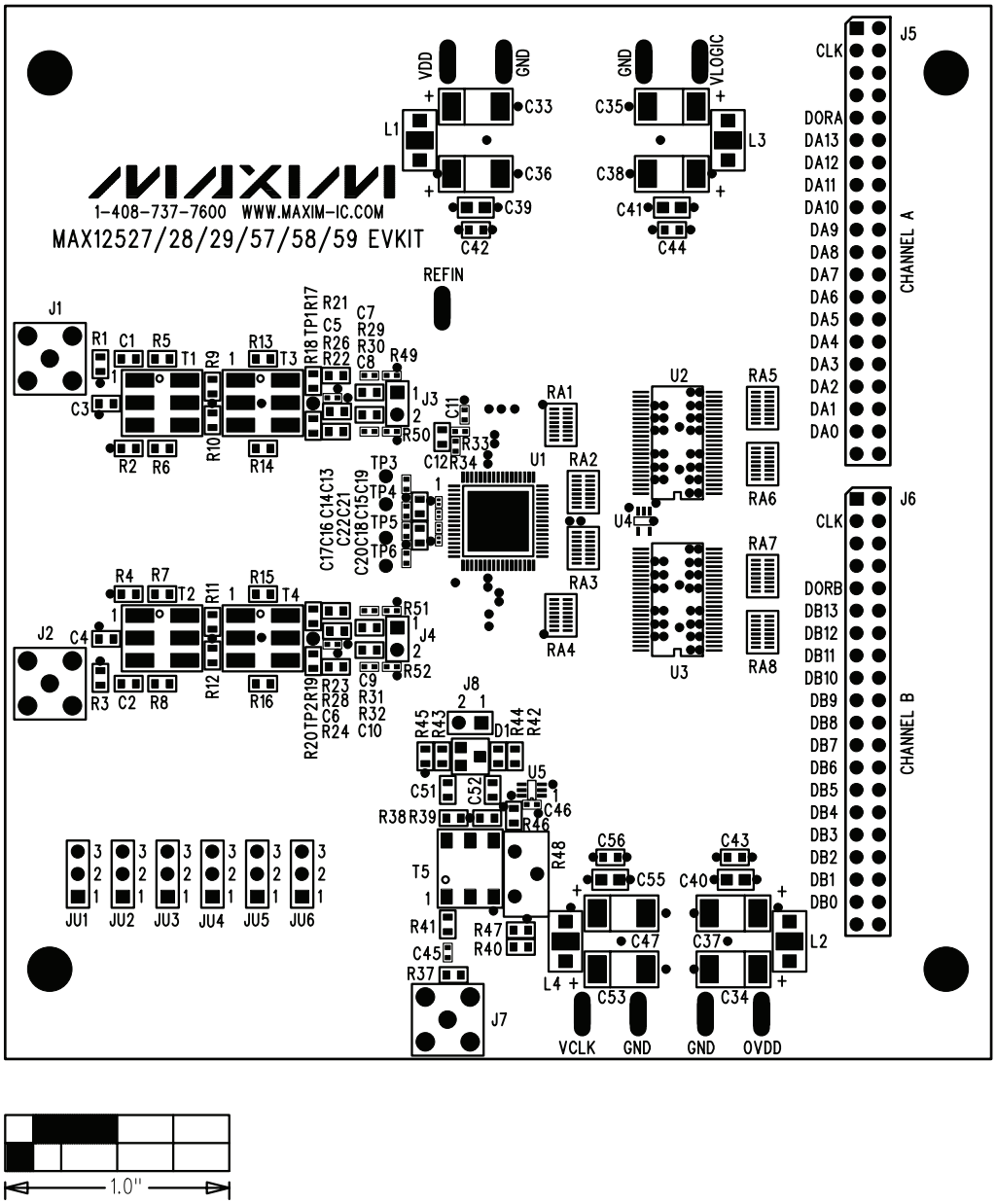

Figure 8. MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV Kit Component Placement Guide—Component Side

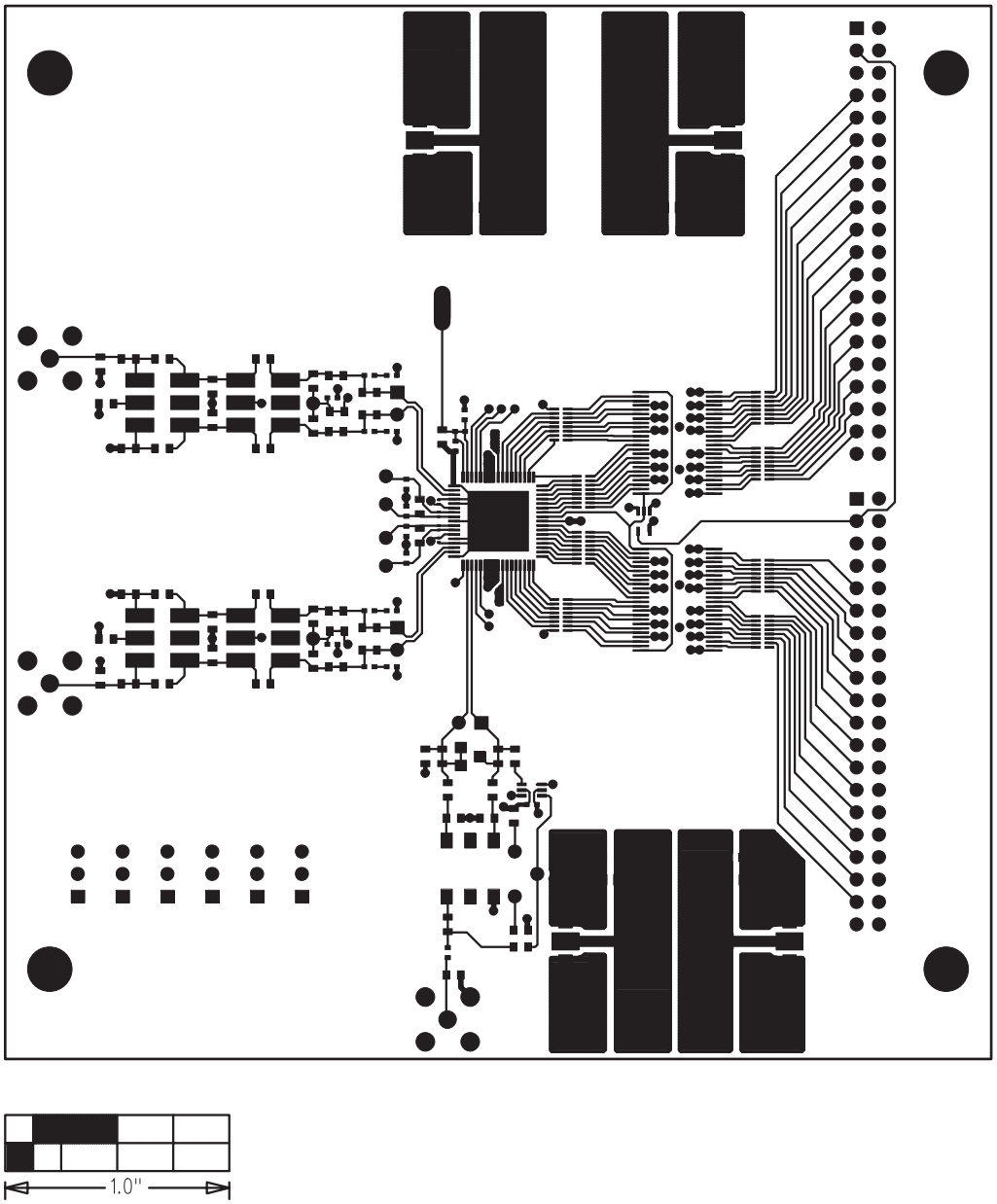

Figure 9. MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV Kit PC Board Layout—Component Side

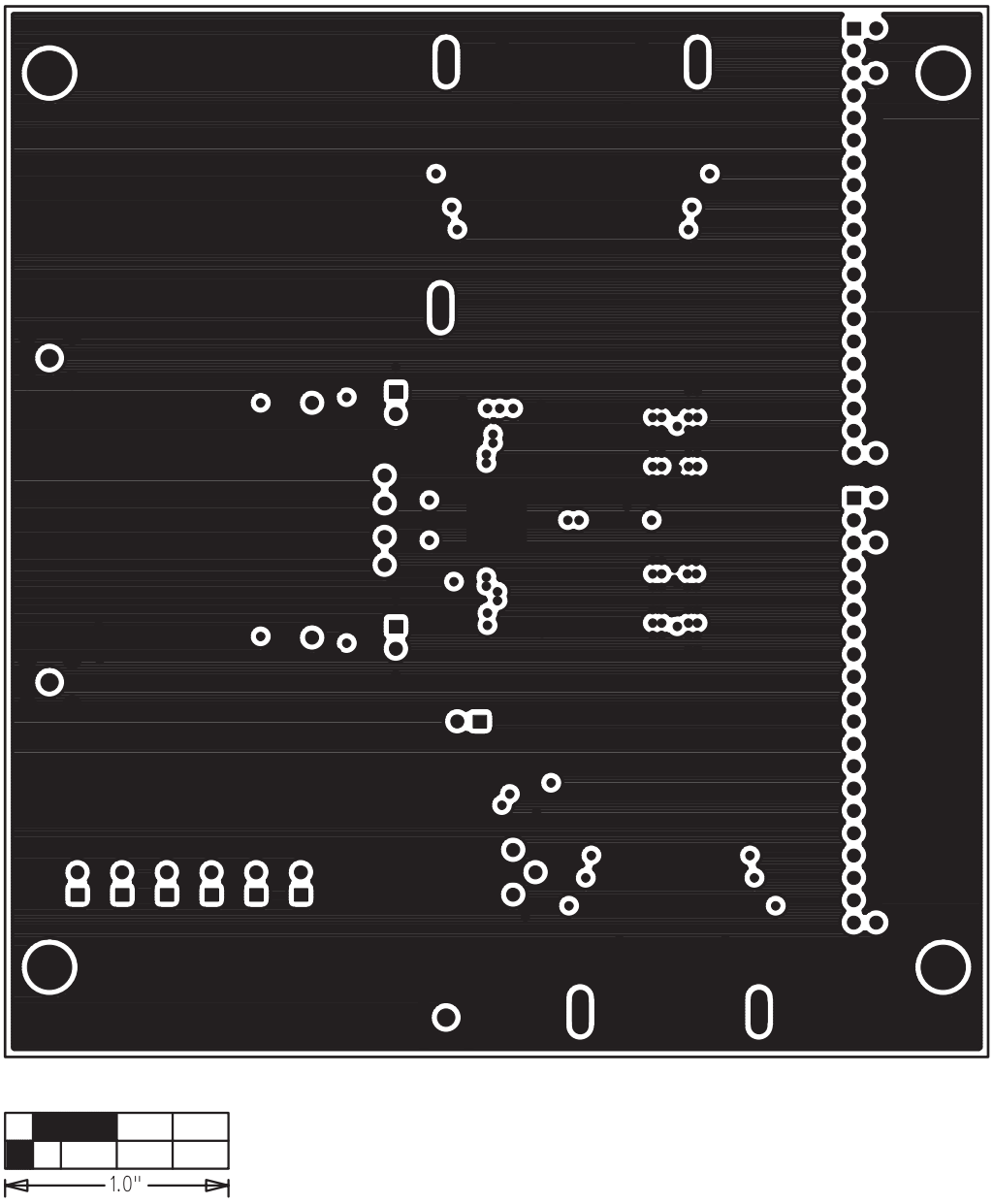

Figure 10. MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV Kit PC Board Layout (Inner Layer 2)—Ground Planes

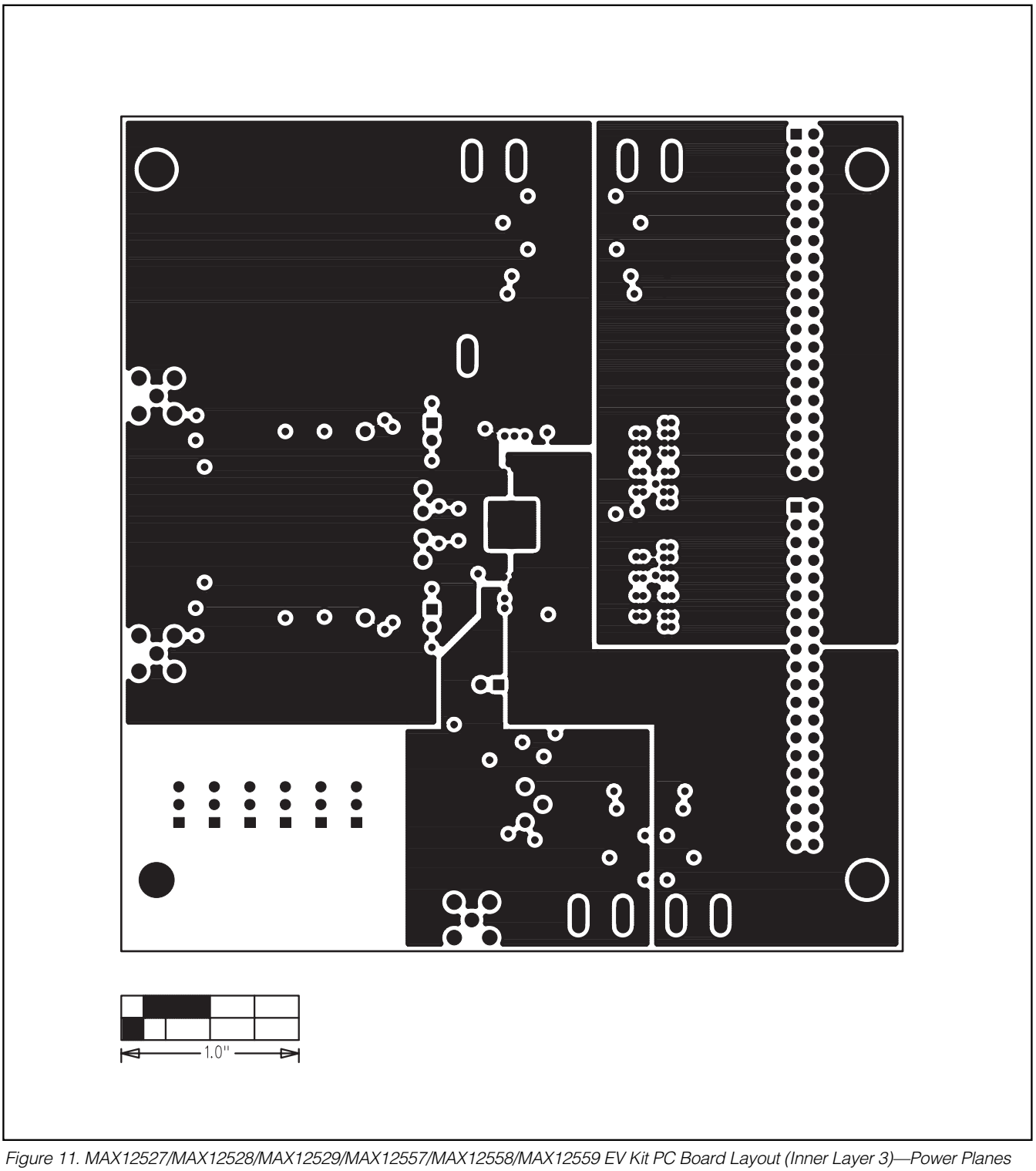

Figure 11. MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV Kit PC Board Layout (Inner Layer 3)—Power Planes

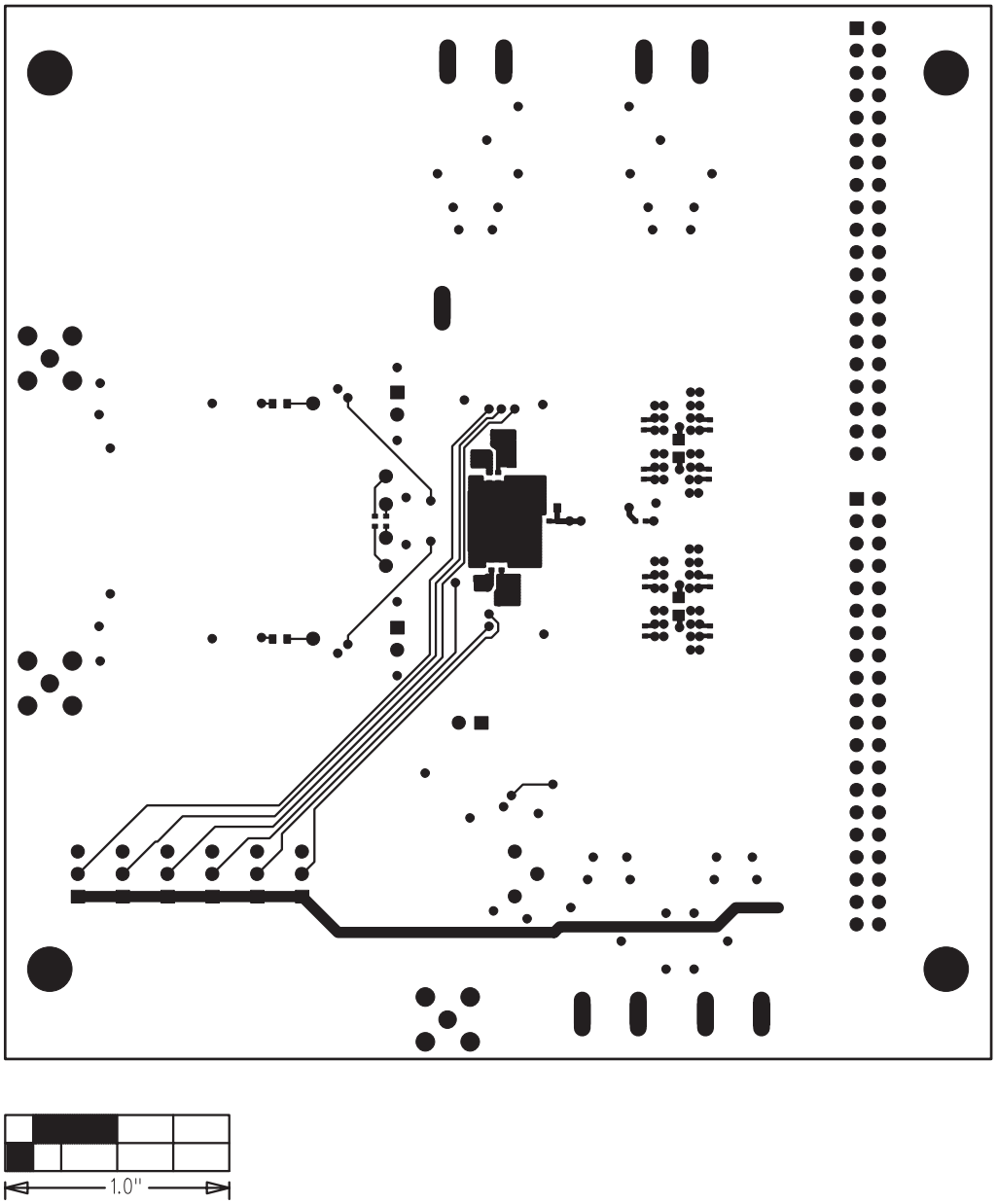

Figure 12. MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV Kit PC Board Layout—Solder Side

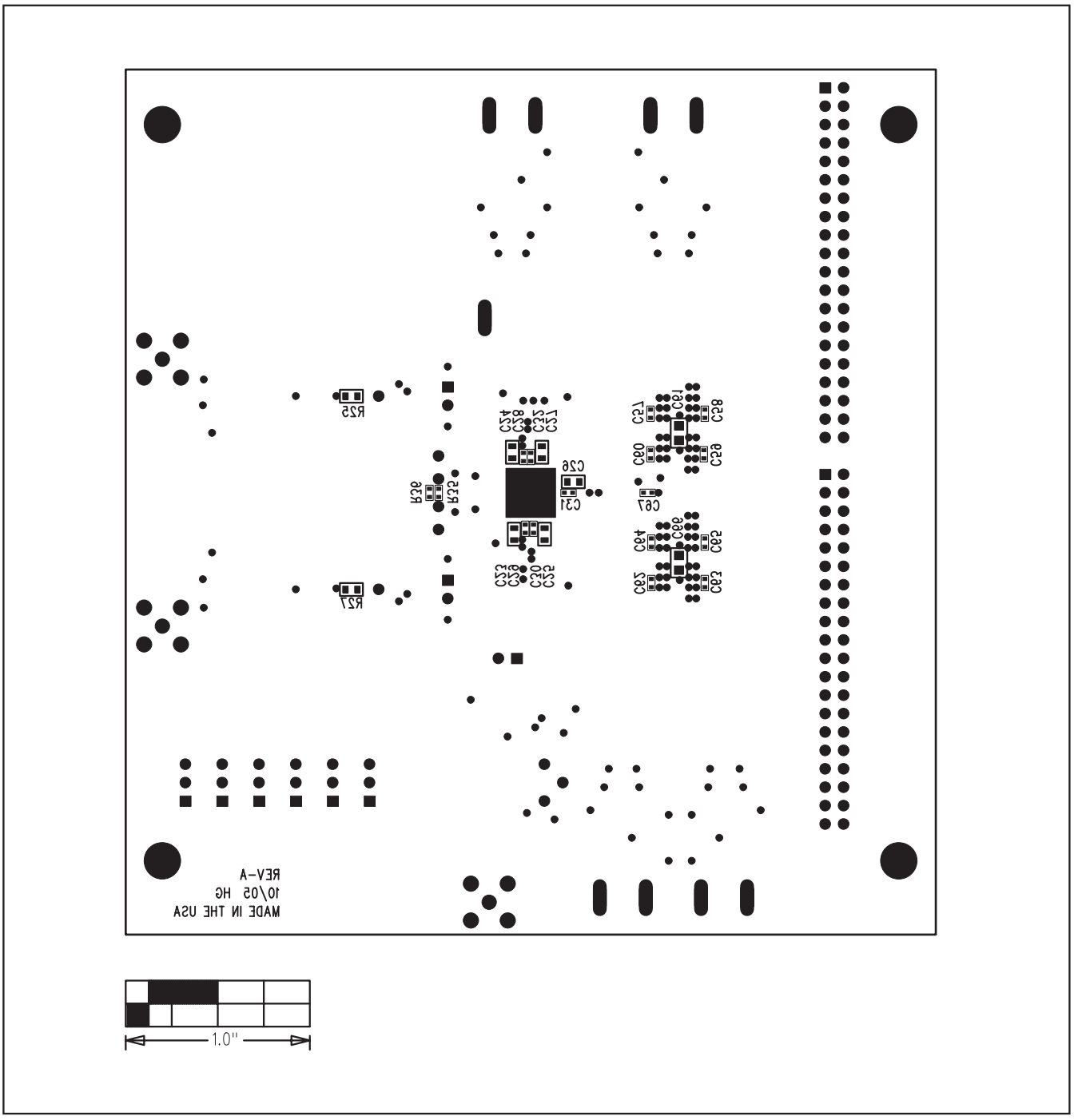

Figure 13. MAX12527/MAX12528/MAX12529/MAX12557/MAX12558/MAX12559 EV Kit PC Board Component Placement Guide—Solder Side